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Effects of Si Recess Structure on Performance and Reliability in High Voltage n-MOSFETs

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Abstract

Device characteristics and hot-carrier reliability of high voltage n-MOSFETs with various Si recess depths introduced by sidewall spacer over-etch are investigated. Experimental results show that the depth of Si recess has small effect on device characteristics. A device with a deeper Si recess has a smaller substrate current but produces a greater hot-carrier degradation. TCAD simulation results suggest that this unexpected result is caused by the severity in plasma damage during sidewall spacer over-etch and the difference in topology.

1. Introduction

It has been reported that plasma-induced Si recess structure has impact on the threshold voltage (V_t) of advanced nMOSFETs [1]. Previous studies discussed this issue by theoretical analyses and TCAD simulations. In this paper, the effects of Si recess structure introduced during sidewall spacer etching process on device characteristics and hot-carrier reliability of high-voltage n-MOSFETs are discussed. Both experimental data and TCAD simulation results are presented and analyzed.

2. Experimental Methods

The schematic cross section of the high-voltage n-type MOSFETs used in this study is shown in Fig. 1. To achieve the required off-state breakdown voltage, the lengths of poly-gate and N^- drift region (L_d) are roughly 0.9 μm and 0.7 μm, respectively. The gate oxide thickness is about 40 nm. Fig. 2 shows the schematic process flow that leads to Si recess structure in this paper. When defining the spacer region after N^- drift implantation and TEOS deposition, Si recess structure is introduced during sidewall spacer etching. The depth of Si recess is mainly affected by the time of over-etch. In this paper, three different depths in Si recess (roughly 5~20 nm) are fabricated and denoted by device A, B, and C. Device A has the shallowest recess depth and device C has the deepest recess depth. Device characteristics including, linear-region drain current (I_{Dlin}), saturation-region drain current (I_{Dsat}), maximum transconductance (G_{mmax}), and V_t are measured. I_{Dlin} is measured at drain voltage (V_D) of 0.1 V and gate voltage (V_G) of 3.3V. I_{Dsat} is measured at $V_G = V_D = 3.3$V. G_{mmax} and V_t are extracted at $V_D = 0.1$ V. The hot-carrier stress is applied under V_D = 10~12 V at the V_G that produces the peak substrate current (I_{sub}). Stress tests are interrupted periodically to measure the degradation of the device.

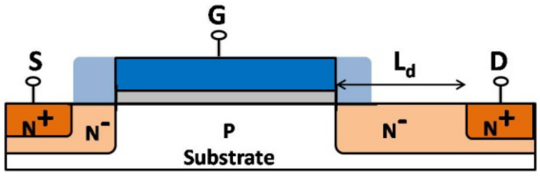

Fig. 1 Schematic cross section of the device used in this paper.

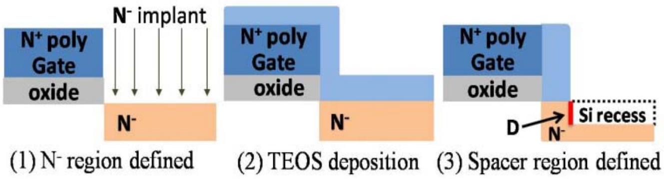

Fig. 2 Schematic process flow that leads to Si recess structure.

3. Results and Discussions

The effects of Si recess on device characteristics are shown in Fig. 3, where I_D-V_G characteristics of devices A, B, and C measured at $V_D = 0.1$ V are shown. The difference in I_D-V_G curves is small, indicating that I_{Dlin}, G_{mmax}, and V_t are almost the same. I_D-V_G measured at $V_D = 3.3$ V (data not shown) also shows small difference in I_{Dsat}. Results mentioned above reveal that the depth of Si recess has small effect on device characteristics in our devices.

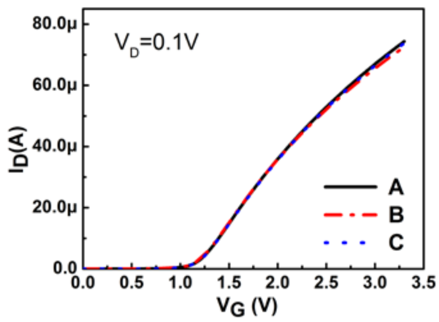

Fig.3 I_D-V_G curves of devices with various depths in Si recess.

To examine hot-carrier reliability of the device, I_{sub}-V_G characteristics of devices are measured at $V_D = 10$ V and shown in Fig. 4. The peak I_{sub} occurs at V_G around 2.9 V. It is clear that a deeper Si recess (recess A < B < C) results in a smaller I_{sub}. Fig. 5 shows the I_{Dlin}, I_{Dsat}, and G_{mmax} degradation of device A stressed under $V_D = 10$ V and $V_G = 2.9$ V (peak I_{sub} condition) for 1000 seconds. I_{Dlin} degrades the most, suggesting that hot-carrier induced damage is mainly located in the N^- region [2].

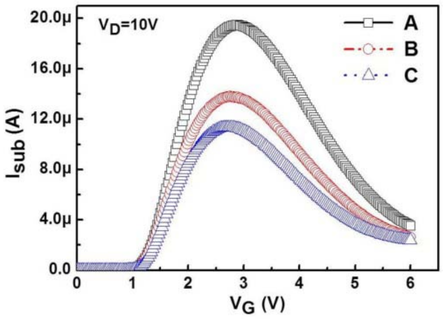

Fig. 4 I_{sub}-V_G curves of devices with various depths in Si recess.

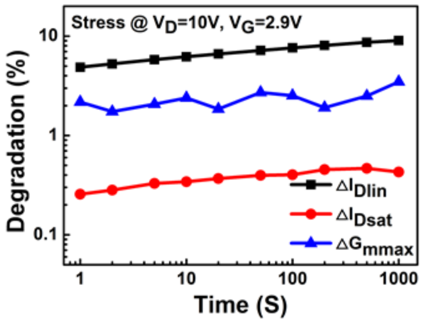

Fig. 5 I_{Dlin}, I_{Dsat}, and G_{mmax} degradation of device A under hot-carrier stress.

The effect of Si recess depth on hot-carrier induced degradation is shown in Fig. 6, where I_{Dlin} degradation of devices stressed under V_D = 10 V and V_G = 2.9 V is compared. A deeper Si recess results in a larger I_{Dlin} degradation. The inset of Fig. 6 shows the device lifetime vs. $1/V_D$, where lifetime is the time to reach 10% I_{Dlin} degradation. It is also clear that a deeper Si recess results in a shorter lifetime. Since I_{sub} value is usually used to judge the severity of device degradation [3], results shown in Fig. 6 is unexpected. In other words, device C has the largest I_{Dlin} degradation even though its I_{sub} is the smallest as in Fig. 4.

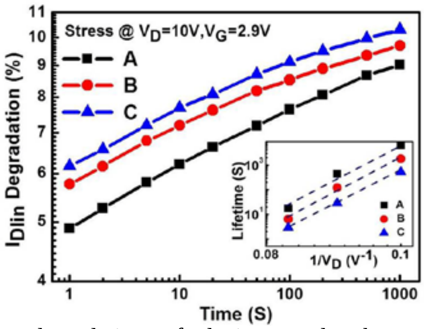

Fig. 6 I_{Dlin} degradation of devices under hot-carrier stress. Hot-carrier lifetime vs. $1/V_D$ is shown in the inset.

To investigate such an unexpected result, calibrated TCAD simulations are performed. Fig. 7 shows the impact ionization (I-I) rate of devices A and C biased at V_D = 10 V and V_G = 2.9 V (the stress condition in Fig. 6). The I-I rate of device A is larger than device C, which is consistent with I_{sub} data in Fig. 4. Besides, the maximum I-I rate occurs under the spacer, i.e. in the N^- drift region, which supports our previous argument that hot-carrier induced damage is mainly located in the N^- region. To evaluate the impact of hot-carrier induced damage on I_{Dlin} degradation, Fig. 8 shows the simulation results of I_{Dlin} degradation vs. hot-carrier induced interface state (N_{it}), where acceptor-type N_{it} is assigned near the Si-SiO_2 interface at the location where maximum I-I rate occurs (as in Fig. 7). From the stress result of device A at t = 1000 s in Fig. 6 (9.0% I_{Dlin} degradation), it can be estimated from Fig. 8 that hot-carrier induced N_{it} during stress is 9.6×10^{11} cm^{-2} in device A. For device C at t = 1000 s in Fig. 6 (10.3% I_{Dlin} degradation), Fig. 8 reveals that N_{it} produced in device C is 9.5×10^{11} cm^{-2}. Such a result leads to the following two inferences. Firstly, during stress device C produces almost the same N_{it} as in device A but device C has much smaller I_{sub} as in Fig. 4. This may cause by the fact that traps are easier to create (near left-side of Si recess area denoted by D in Fig. 2) in device C due to more direct plasma interaction [4] during sidewall over-etch. Secondly, for the same amount of N_{it}, device C produces a larger I_{Dlin} degradation. This may cause by the topology difference such that the impact of N_{it} on I_{Dlin} degradation is enhanced in a device with a deeper Si recess. From the above analyses, it is inferred that the larger hot-carrier degradation in a device with a deeper Si recess is caused by more plasma damage and the topology difference.

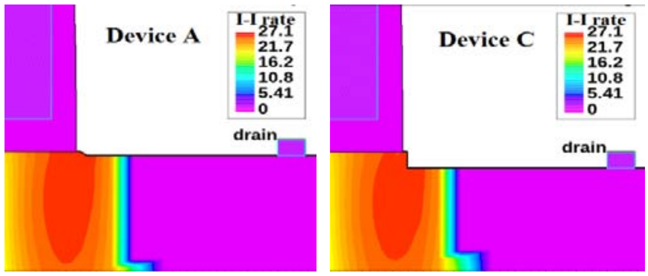

Fig. 7 I-I rate contour of devices A and C bias at stress condition.

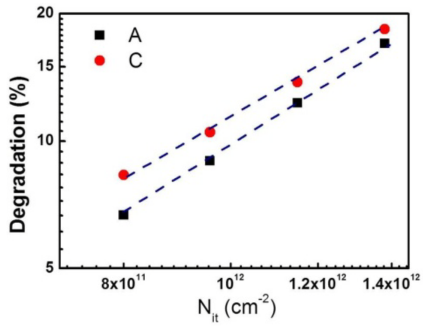

Fig. 8 The impact of hot-carrier induced N_{it} on I_{Dlin} degradation.

4. Conclusions

The device characteristics and hot-carrier reliability of high voltage n-MOSFETs with various Si recess depths introduced by sidewall spacer over-etch are presented. Results show that the depth of Si recess has small effect on device characteristics. A device with a deeper Si recess has a smaller I_{sub} but produces a greater hot-carrier degradation unexpectedly. Our analyses suggest that the severity of plasma damage during sidewall spacer over-etch and the topology difference lead to this unexpected result.

References

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