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Hot-carrier Induced Drastic Off-state Leakage Current Degradation in STI-based N-channel LDMOS

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Abstract

In this paper, hot-carrier (HC) induced drastic off-state leakage current (Ioff) degradation for the LDMOS is found and the mechanism is also investigated in detail. Continuous on-state drain current flow of the LDMOS generates the HC which is trapped in the STI, and causes the drastic increase of the Ioff for the LDMOS. Therefore, HC induced drastic Ioff increase should be taken into account for the LDMOS design.

1. Introduction

With scaling down the device size, shallow trench isolation (STI) has been commonly used in LDMOS. Low on-resistance (Ron) and high breakdown voltage can be achieved by utilizing STI [1]. However, the STI structure also causes and enhances HC induced degradation due to trapped charge in the STI region. It has been widely known that the trapped charge in the STI caused threshold voltage (Vth) and breakdown voltage (BVdss) change [2], and a few papers reported Ron and drain current degradation [3]. In this paper, HC induced off-state current degradation for the LDMOS is reported and the mechanism is also investigated. To improve IC's consumption current and life time, understanding the mechanism of the drastic Ioff degradation and feedback it into the LDMOS design is indispensable.

2. Device Structure and Experiments

In this paper, the device was fabricated by using 0.13µm CMOS-DMOS technology [4]. Cross-sectional view of 40V n-ch LDMOS is shown in Fig. 1. The degradation under HC stress condition was measured as a function of off-state drain-source leakage current (Ioff). We also utilized the 2D-TCAD simulation to analyze the results.

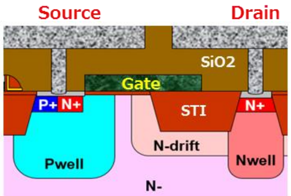

Fig. 1. Cross-sectional structure of 40V n-ch LDMOS.

3. Electrical Characteristics and Discussion

Fig. 2 shows measured Ioff of 40V n-ch LDMOS during HC stress (Vg=2V, Vd=46V). Ioff drastically increased more than three decades after a certain stress time and then saturated.

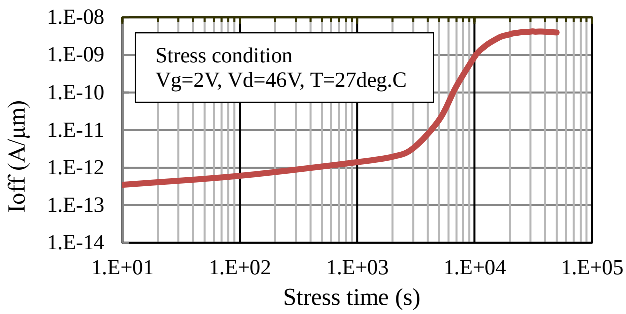

Fig. 2 Measured Ioff of 40V n-ch LDMOS during HC stress.

For further understanding, the off-state drain current to each electrode was measured by using the device as shown in Fig. 3, in which source and back-gate is electrically separated by STI. Measured curves of the initial device (Fig. 4 (a)) and the device after HC stress (Fig. 4 (b)) indicated that the leakage current from drain flew into the back-gate neither into the source nor the gate.

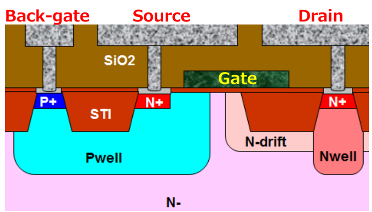

Fig. 3 Cross-sectional structure of 40V n-ch LDMOS which has isolated back-gate and source structure.

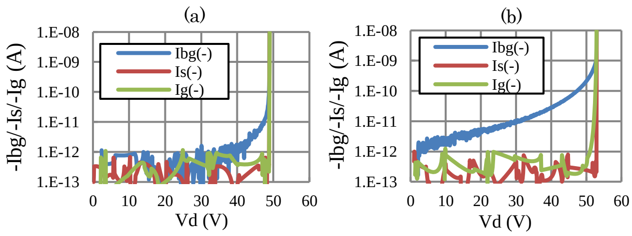

Fig. 4 Measured I-V characteristics for back-gate current (Ibg), source current (Is) and gate current (Ig) of the devices at Vg=0V, (a) initial and (b) after HC stress of 1E+4s.

Moreover, the current between the drain and the back-gate was dominant even after the Ioff-increase. Based on these results, it was assumed that the Ioff increase has occurred not because of the HC injection into gate oxide which results in Vth change or gate oxide destruction.

Meanwhile, stress gate voltage dependence of the Ioff increase was also measured (Fig. 5).

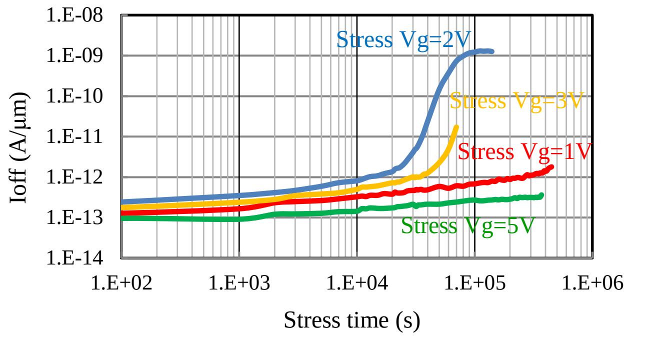

Fig. 5 Stress time dependence of measured Ioff of 40V n-ch LDMOS as a function of stress gate voltage (Stress Vg).
HC stress: Vd=40V, T=27deg.C.

It was confirmed that the drastic Ioff increase occurred in the shortest time when Vg=2V. In order to understand these results, the impact-ionization was simulated by 2D TCAD as shown in Fig. 6. It is shown that impact-ionization mainly occurred at STI edge when Vg=2V.

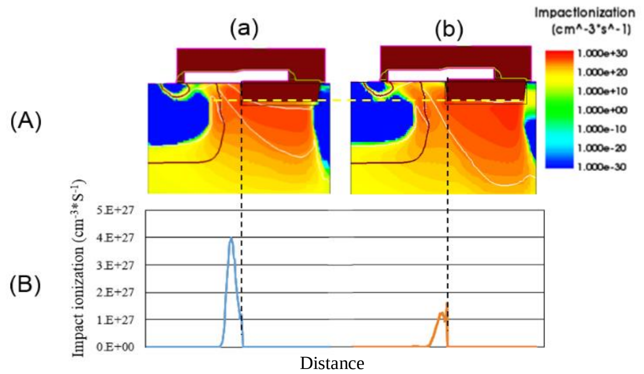

Fig. 6 Simulated results of impact-ionization rate 2D distribution (A) and its 1D profile at STI edge (B), under stress condition of (a) Vg=2V, Vd=40V and (b) Vg=5V, Vd=40V.

Accordingly, it is recognized that the on-state drain current flow of n-ch LDMOS toward the STI edge causes the HC generation and creates the fixed charge at the STI/Si interface. For further understanding, the HC induced fixed charge influence on off-state leakage current was also investigated by the simulation. In the simulation, the fixed charge was put along STI/Si interface (Fig. 7) and the amount of the fixed charge was varied.

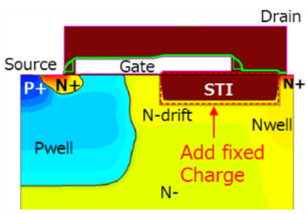

Fig. 7 2D-TCAD simulated device structure with fixed charge along STI/Si interface.

Fig. 8 shows the simulated results of impact-ionization distribution under off-state conditions as a function of the amount of fixed charge. It is noted that as increasing the fixed charge at the STI/Si interface, the impact-ionization occurred and increased due to electric field enhancement by fixed charge at STI edge even under the off-state condition.

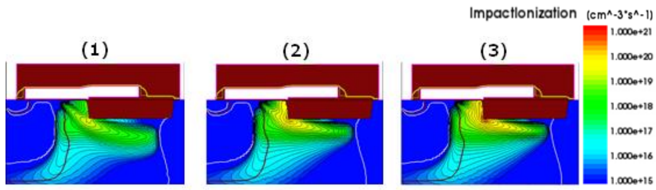

Fig. 8 TCAD simulation results of impact-ionization during off-state condition (Vg=0V, Vd=40V) with the fixed charge along STI/Si interface (1) no charge, (2) 6E11 cm^{-2} and (3) 7E11 cm^{-2}.

Based on these results, it is assumed that the continuous HC injection increases the fixed charge at the STI/Si interface and results in drastic Ioff increase, eventually. To confirm this assumption, off-state leakage current was also simulated as shown in Fig. 9.

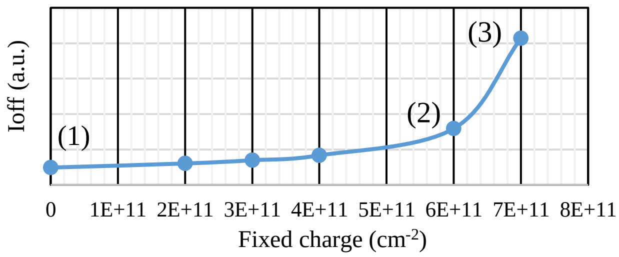

Fig. 9 Simulated Ioff dependence of the fixed charge along STI/Si interface. The numbers correspond to Fig. 8.

It was clearly shown that the Ioff increased as the fixed charge increased and drastically increased when the fixed charge amount exceeded 4E11 cm^{-2}. These simulated results are well corresponded to the measured results.

In LDMOS design, this phenomenon should be considered and drift region optimization with STI structure is important.

4. Conclusions

In this work, the mechanism of HC induced drastic off-state leakage current increase for the LDMOS is investigated in detail. This drastic increase of Ioff might have a serious impact on circuit operation, and to prevent this phenomenon, careful drift layer optimization with STI shape is indispensable for LDMOS design.

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