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# Experimental Investigation of Localized Stress Induced Leakage Current Distribution in Gate Dielectrics Using Array Test Circuit

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**Abstract**

**In this study, SILC distributions were measured from with a large number of MOSFETs with various gate area using array test circuit. It was found that a spot with the largest SILC within each gate area dominates its total current, and the SILC values of these individual spots do not scale, leading to a severe impact to scaled devices such as flash memories.**

## 1. Introduction

Stress Induced Leakage Current (SILC) causes a severe limitation of the scaling down of flash memory, because the number of stored charges decreases, and a thinner oxide results in a larger SILC [1]. Especially, anomalously large SILC which appears on a local spot causes bit errors [2]. It is essentially important to clarify the SILC distribution of these individual spots in order to reduce the large SILC components. A statistical SILC measurement system using array test circuit was reported [3]. With this measurement system in Fig. 1, the gate current down to the order of $10^{-17}$A of over 80k MOSFETs are measured within 80sec. In this study, SILC distributions of a large number of MOSFETs with different gate area are measured, and the localized SILC distribution is analyzed to investigate SILC defect distribution.

## 2. Experimental Setup

Table I shows the specifications of the measured samples, stress induction, and SILC measurement conditions. SILC of a large number of NMOS transistors with three types of gate area (1×1 μm$^2$, 0.5×0.5 μm$^2$, 0.25×0.25 μm$^2$) were measured. The measurements were carried out at -30°C in order to accurately measure gate current down to $10^{-17}$A [4]. The measured samples were fabricated by a 0.18μm 1Poly - 3Metal CMOS technology. The gate oxide thickness was 5.5 nm. The number of samples was 10,440 for 1×1 μm$^2$ size, and 20,880 for other two sizes. To each sample, a series of oxide field ($E_{OX}$) stress from 9.0MV/cm to 11.0MV/cm with 0.5MV/cm step was applied. The time was 1000 s for each $E_{OX}$ stress. The applied $E_{OX}$ while measuring SILC was varied from 0 to 8.1MV/cm with 0.05MV/cm step.

## 3. Results and Discussion

Fig. 2 shows the average gate current density ($J_G$)-$E_{OX}$ characteristics of the measured samples. Almost the same characteristics were obtained for the three gate sizes, indicating the average current density is normalized by the gate area.

However, by analyzing SILC characteristic of each MOSFET, some transistors with very large SILC were detected. Fig. 3(a-c) shows the absolute current ($I_G$)-$E_{OX}$ characteristics of the transistors with large SILC. These SILC values are several orders of magnitude larger than the average values, especially in lower $E_{OX}$ range, leading to a severe impact in flash memory. Also, these SILC values are within the same orders nevertheless the gate area is 16 times different at most. In addition, for some transistors, drastic changes of SILC like random telegraph signals appear, indicating that these SILC are due to individual spots.

Fig. 4(a) shows the Gumbel plots of the SILC after stress of 9.5 MV/cm-1000 sec, measured at 6.8 MV/cm. The distributions are on the straight lines in the large SILC region for each curve. It was reported that these characteristics indicate the SILC after a relatively low intensity stress is generated by one localized leakage spot in each MOSFET [4]. In TDDB characteristics, the definition of defect density per unit gate area using Poisson distribution was reported [5]. Likewise, the density of the defect that generates certain SILC is defined with the following equation [6].

$$P = \exp\left(-A \cdot D_{SILC}\right) \qquad (1)$$

Where P is cumulative probability, A is gate area, and $D_{SILC}$ is cumulative defect density generating certain SILC per unit gate area. With the assumption that $D_{SILC}$ is equal among the different gate area, the localized current distribution can be normalized by the following equation.

$$P_1 = P_2^{A_1/A_2} \qquad (2)$$

Fig. 4(b) is the result of the normalization using eq. (2). The overlapped line in high SILC region indicates the localized SILC distribution is normalized by the introduced SILC defect density. Fig. 4(c) shows SILC density distribution normalized by gate area. Obviously, measured curves are different among different gate area, supporting the SILC values do not scale by the gate size.

Fig. 5(a) shows the calculated SILC defect density obtained by taking the differential of $D_{SILC}$ by $I_G$. In Fig. 5(a), SILC defect density distribution of the three types of gate area are almost the same when $I_G$ is higher than $10^{-16}$A. From this result, a schematic diagram of SILC defect distribution in a gate area is illustrated as shown in Fig. 5(b). The number of defects generating $10^{-17}$A SILC is about 100 in a gate area of 10,000 μm$^2$. Likewise, the number of defects generating $10^{-15}$A SILC is about 20 in the same gate area. The obtained SILC defect density is very important to characterize the gate oxide quality for scaled devices including flash memories.

## 4. Conclusion

SILC distributions in a large number of MOSFETs with various gate area were measured and statistically analyzed. It was verified that a spot with the largest SILC within each gate area dominates its total current in small size MOSFETs, and the SILC values of these individual spots do not scale with gate size. The distribution of SILC defect density was experimentally obtained for the fabricated devices, which is to be useful for the characterization of flash memories.

## References

[1] K. Naruke, et al., IEDM, p.424 (1988).
[2] F. Arai, et al., IRPS, **66**, p.378 (1998).
[3] Y. Kumagai et al., IEEE Trans. Electron Devices, **58** (2011).
[4] T. Inatsuka et al., IRPS, GD.5 (2013).
[5] A. Teramoto et al., Microelectronics Reliability, **41** (2001).
[6] H. W. Park et al., IRPS, DG-7 (2017).

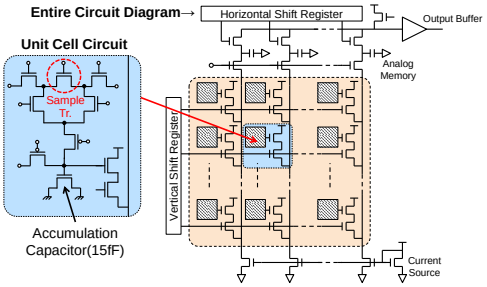


Fig. 1 Circuit diagram of array test circuit.

Table I Sample specifications and the SILC measurement conditions.

| | | | |
|---|---|---|---|
| Gate Area (WxL) | 1x1 μm² | 0.5x0.5 μm² | 0.25x0.25 μm² |
| No. of Samples | 10,440 | 20,880 | 20,880 |
| Sample Type | NMOS Transistors | | |
| Oxide Thickness | 5.5 nm | | |
| Technology Node | 0.18μm CMOS with 1Poly - 3Metal | | |
| Stress Condition | 9.0MV/cm-1000sec → 9.5MV/cm-1000sec →10.0MV/cm-1000sec → 10.5MV/cm-1000sec →11.0MV/cm-1000sec | | |
| $E_{OX}$ for measurement | From 0 to 8.1MV/cm (0.05 MV/cm step) | | |

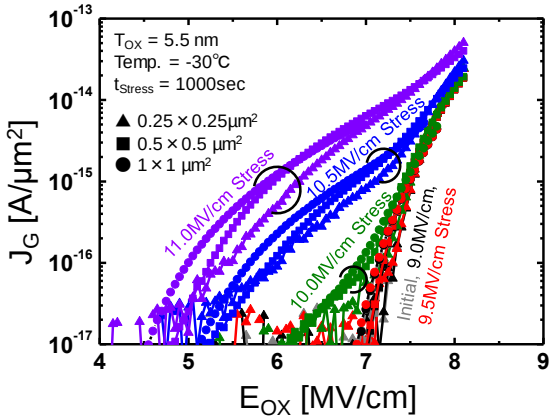


Fig. 2 Average $J_G$-$E_{OX}$ characteristics of the number of more than 10,000 NMOS transistors with various gate area and the stress conditions. When $I_G$ is normalized with current density, the SILC with each stress condition shows almost the same characteristics.

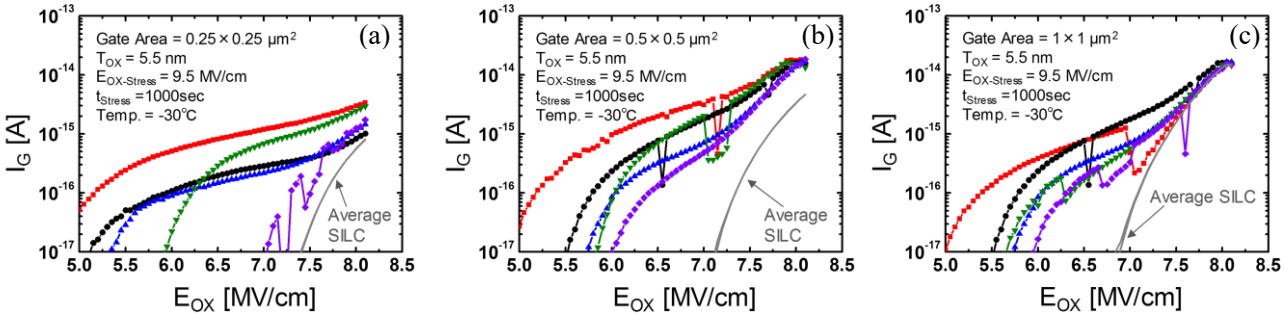


Fig. 3 Comparisons between the average SILC and the $I_G$-$E_{OX}$ curves of five large SILC cells with the respective gate area of (a) 0.25×0.25 μm², (b) 0.5×0.5 μm² and (c) 1×1 μm².

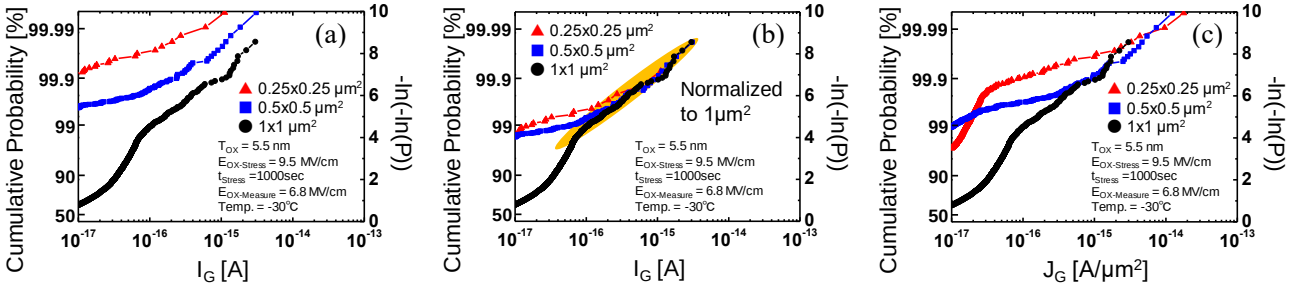


Fig. 4 (a) Gumbel Plots of the samples with three types of gate area in a specific stress condition and $E_{OX}$, and the results of the normalization with (b) the defect density, (c) current density.

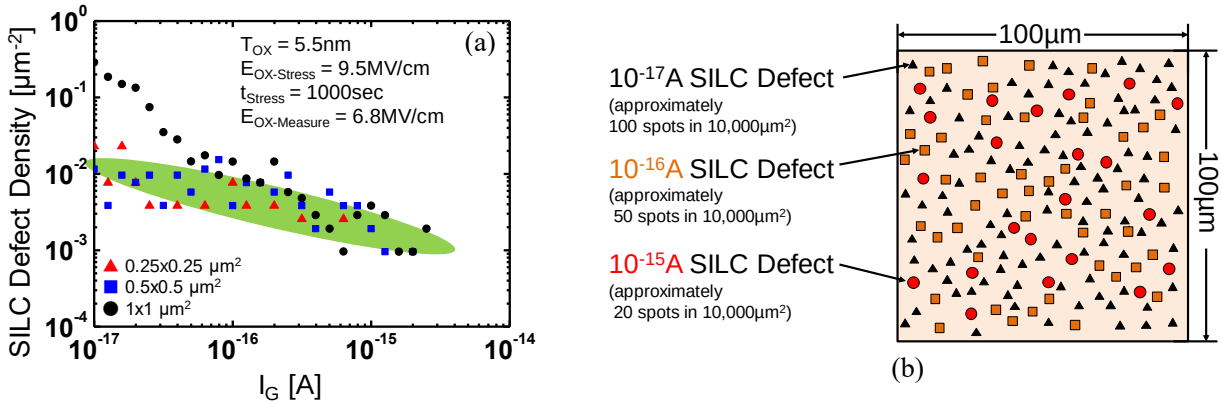


Fig. 5 (a) Calculated SILC defect density from Fig. 4(b) and (b) schematic diagram of considered SILC defect distributions.