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Impact of Mechanical Stress to Cell Characteristics in Vertically Stacked NAND Flash Structure

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Abstract

The stress distribution and the impact of them to cell characteristics are investigated in vertically stacked NAND flash memory. It is revealed that the stress of contact hole depends on the distance from the tungsten common source line(CSL) slit, which changed the NAND cell characteristics more than 4% respectively. Therefore, position of channel hole contact affects the uniformity of the NAND cell taking into consideration the mechanical stress and should be considered in cell design.

1. Introduction

Three dimensional (3D) NAND flash memory has been developed as the most promising architecture for high demand of storage capability because of its high density and improved performance compared to previous 2D type. 3D NAND memory technology has been developed through the scaling down the numerical parameters and stacking the cell for better integration. However, new structure with high stacking as well as complex process step make an unsuspected issue such as mechanical stress, critical dimension (CD) variation and, cell-to-cell interference. Especially mechanical stress caused by mismatch in 3D multilayer and thermal fabrication process such as high stack patterning, WL recess-refill, high stack etching lead to structural problem and degradation of electrical characteristics [1]. Stress also modified the silicon band structure with poly-Si channel, which make a cell uniformity distortion and severe reliability issues. Therefore, control the stress in multi-layer is critical issue in 3D NAND architecture and mitigate the effect of stress is key point to get a better stable cell performances.

In this work, the effect of stress in vertically stacked NAND structure was discussed. Particularly, we investigated the distribution of stress by the tungsten common source line (CSL) slit and the effect of stress in cell characteristic was studied.

2. Simulation Methodology

To analyze the effect of stress in 3D NAND, we used the Sentaurus TCAD simulator and 3D structure was based on V-NAND [2], which proposed by Samsung Electronics. We performed two channel holes with staggered pillar type and set the 6 WL stacked structure for efficient experiments. In all material, stress parameters such as Young's modulus, Bulk modulus, Shear modulus, and Poisson ratio was applied to TCAD simulator. Furthermore, we focused on the effect of tungsten stress which is elastic material with a relatively high stress value in 3D NAND structure. Figure 1 shows the simulation schematics of the 3D NAND.

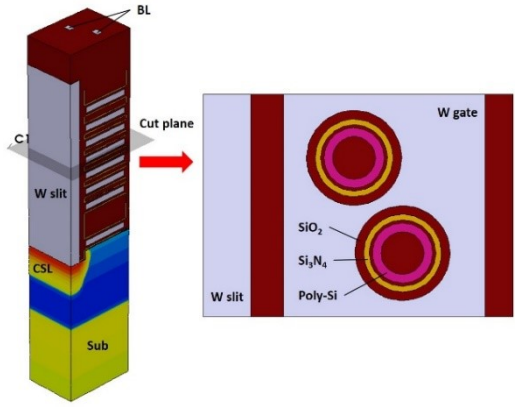

Fig. 1 3D image of the 3D NAND structure and cut plane of vertical axis.

3. Simulation Results and Discussion

To investigate the effect of stress in 3D NAND structure, we observed the vertical direction stress on the section cut into the longitudinal axis. In CMOS device, the strain caused by lattice mismatch affects the silicon band energy, which lead to mobility variation in silicon channel [3,4]. In the case of NMOS, the tensile stress in the channel direction improves the mobility and the PMOS is improved by compressive stress [3,4]. In this respect, we discussed the effect of stress on 3D NAND.

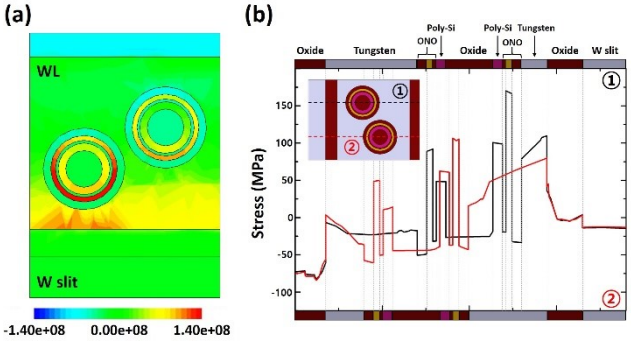

Fig. 2 The (a)stress distribution of the vertical axis cut plane and (b) stress distribution of the cut line at different point.

Figure 2 (a) shows the stress distribution in cross section of the structure. In multi-layer interface, tensile stress arises from lattice mismatch, which was relatively large in near the tungsten CSL slit and alleviated farther away from it. Because the tungsten has relatively large tensile stress compared to other materials constituting the 3D NAND, it transferred tensile stress to inner layer. Figure 2 (b) shows the stress distribution cut in the longitudinal direction at different points. Overall, tungsten, poly-silicon, and silicon-nitride have a tensile stress and silicon-oxide have a compressive stress and the both stress distribution show the similar tendencies. However, each channel hole has different stress value depending on the position; channel near the tungsten CSL slit has high value of stress.

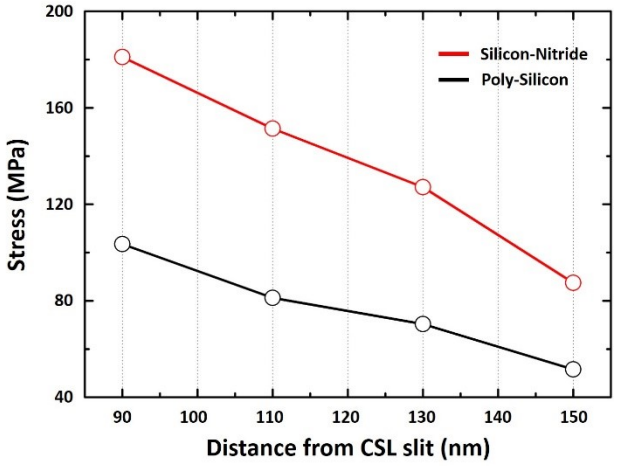

Fig. 3 The average stress of poly-Si channel with different channel hole position.

Figure 3 shows the value of average stress on poly-Si channel and silicon-nitride trap layer at different distance from tungsten CSL, which represents a decreasing tendency with the increasing of distance from CSL slit. When the channel hole position at a distance from CSL slit changed from 90 to 150 nm, the value of average stress was changed to approximately one-fifth of stress value in 90 nm, which means that poly-silicon channel and silicon-nitride trap layer average stress also drastically changed depending on the contact hole position.

To evaluate the effect of stress on cell characteristics, the reading operation was conducted. We proceed separately in case of considering stress model and not in case of stress model, thereby the effect of stress on electrical characteristics was investigated. Figure 4 shows the I-V cell characteristics and rate of variation with the different position from the CSL slit. As shown in figure, all of them shows the current variation under the tensile stress, but the rate of change depends on the applied stress value respectively. In terms of rate of current variation, NAND cell 90 nm away from CSL slit shows the approximately 2 times larger value than cell 150 nm away from CSL slit, which means that the cell uniformity was reduced by the effect of mechanical stress.

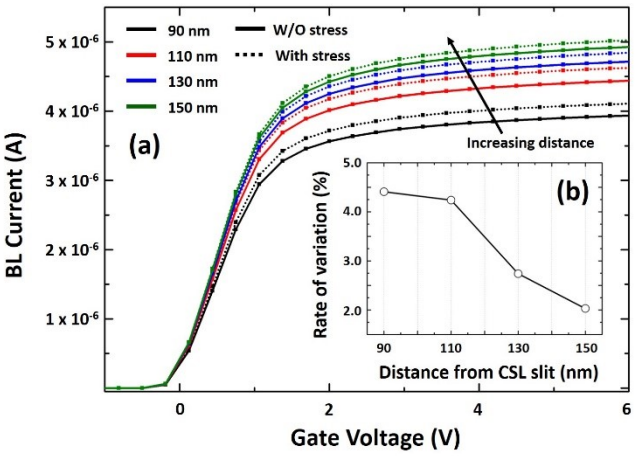

Fig. 4 The (a) I-V characteristics and (b) rate of variation with different channel hole position.

The effect of stress induced by tungsten CSL slit was depending on the position of channel hole, which was the one of the critical issue to obtain the cell uniformity in 3D NAND flash memory.

3. Conclusions

In this work, the impact of mechanical stress to NAND cell characteristics in vertically stacked flash memory was investigated by 3D process simulation method in terms of geometrical parameters. The tungsten CSL slit exhibited the stress transferring to surrounding film due to its relatively large tensile stress in 3D NAND, which caused a stress imbalance in the channel hole at different position. About 4% or more in cell characteristics variation occurs in a channel located in different position, which reduces the NAND cell uniformity. In view of mechanical stress, the position of the channel hole can be critical issue and should be well controlled for NAND cell uniformity in recently staggered pillar type.

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