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New Tunnel FET Charge-Trapping Memory with Large Memory Window for Ultra Low Power Operation

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Abstract

Charge-trapping memory needs a larger memory window for low power operation. Tunnel FET structure is one of the promising structure to achieve the large memory window due to its asymmetric structure. In the case of tunnel FET with N^+ gate, there is higher electric field between P^+ source and N^+ gate edge compared with conventional FET structure. This high electric field enables a large amount of charge injection into the charge storage layer. In this study, we fabricated a SONOS memory with tunnel FET and evaluated write-operation characteristics.

1. Introduction

Charge-trapping memory, like silicon–oxide–nitride–oxide-semiconductor (SONOS) structure, shows stronger scaling ability and higher reliability due to discrete traps in the charge-trapping medium. Charge-trapping memory needs much larger memory window and multi-level operation for low power operation and large memory capacity. Recently, charge-trapping memory with tunnel field-effect transistor (TFET) structure attracts much attention to realize low power operation due to its steep-slope characteristics [1]. On the other hand, TFET has the promising structure to achieve large memory window due to its asymmetric Source/Drain structure. In the case of TFET with N^+ gate, there is higher electric field between the N^+ gate edge and the P^+ source compared with conventional FET structure, as shown in Fig. 1 [2]. Therefore, in the case of the SONOS memory with TFET, more charges are injected in the trapping layer due to this high electric field. In addition, there is a possibility that TFET can achieve more multi-level cells due to its steep-slope characteristics.

In this paper, the SONOS memory with TFET was fabricated, and the width of memory window was evaluated compared with conventional FET structure.

2. Cell structure and electric-field simulation

We proposed the SONOS memory with TFET to realize large memory window due to high electric-field, as shown in Fig. 1. Actually, we investigated the electric field of SONOS memory with TFET and FET structure by TCAD simulation. Figure 2 shows the simulation results of electric field distributions at the source edge when the gate and source/drain voltages are 5 V and 0 V, respectively. In the case of TFET structure, we can observe the high electric field, unlike the conventional FET structure. This high electric field can realize a large amount of charge injection at the overlap region between N^+ gate and P^+ source, as shown in Fig. 3. And, these injected charges act as the most important role for threshold-voltage shift of the TFET, because the electrons tunneled at the source edge.

3. Results and discussion

Figure 4 shows the process flow of the SONOS memory with TFET. After isolation process, B^+ was implanted for threshold-voltage adjustment. Then, oxide-nitride-oxide layer was deposited. After poly-Si gate formation, the P^+ source and the N^+ drain were formed by ion implantation. Finally, Al wiring was formed. Drain current (I_d) - gate voltage (V_g) characteristics of the SONOS memory with FET and TFET are shown in Figs. 5 and 6, respectively. Here, the gate length (L_g) was 1 μm. These I_d-V_g characteristics were measured with V_g from -6 V to 6 V. This drain current was induced by the tunnel effect at the P^+ source edge, as shown in Fig. 7. In the case of TFET structure, the I_d-V_g characteristics obviously shows a large memory window compared with conventional FET structure. Figure 8 shows the relationships between gate sweep voltages and the threshold voltage shift for the SONOS memory with TFET and with FET structure. These results indicate that TFET structure improves the charge injection characteristics due to high electric field at the source edge.

4. Conclusion

We proposed the SONOS memory with TFET structure to realize a large memory window for low power operation. In this paper, the SONOS memory with TFET and conventional FET structure were fabricated. Further, I_d-V_g characteristics were measured. It is observed from the measurement results that TFET structure improves the charge injection characteristics. This can be attributed to the high electric field at the source edge due to its asymmetric structure. All the above results indicated that the TFET was a promising structure to realize a charge-trapping memory with large memory window.

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References

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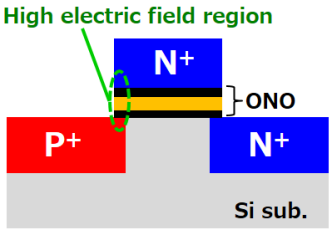

Fig. 1. Schematic of the cross-section of a SONOS memory cell with TFET structure.

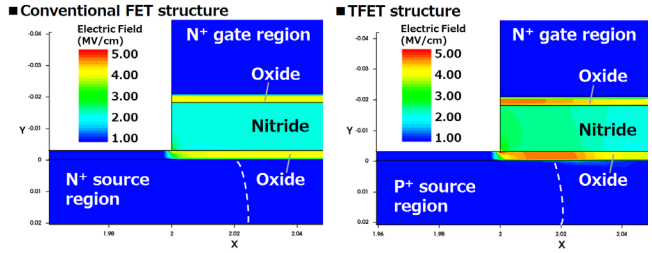

Fig. 2. TCAD simulation results of electric field distributions of SONOS memory devices with conventional FET structure (left) and TFET structure (right).

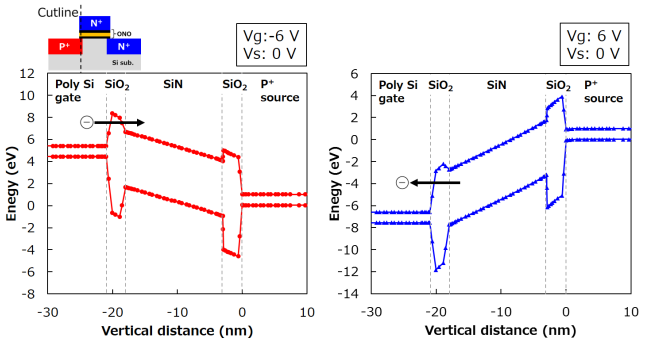

Fig. 3. Energy band diagram of the overlap region between gate and source of the SONOS memory with TFET structure for programming (left) and erasing operation (right).

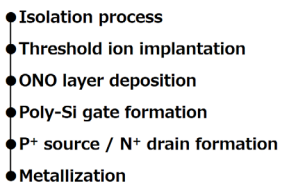

Fig. 4. Process flow of the SONOS memory with TFET.

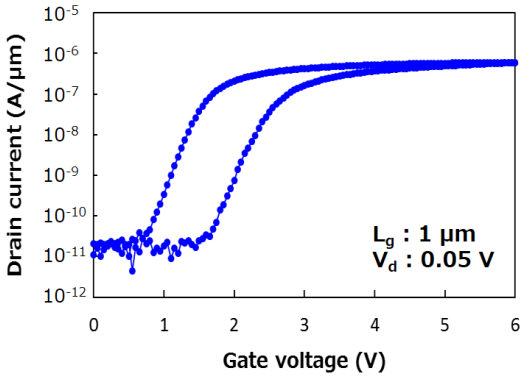

Fig. 5. Measurement results of I_d-V_g characteristics of the SONOS memory with conventional FET structure.

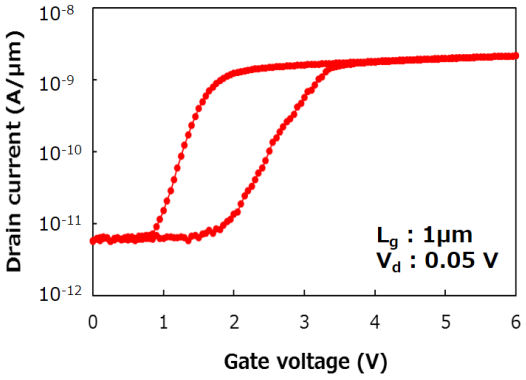

Fig. 6. Measurement results of I_d-V_g characteristics of the SONOS memory with TFET structure.

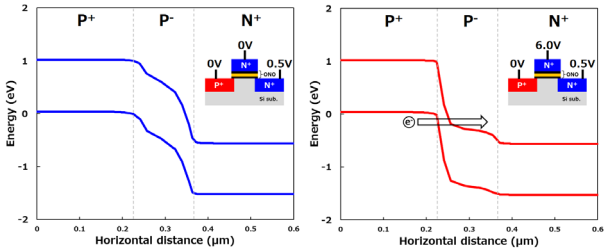

Fig. 7. Energy band diagram along the channel region of the SONOS memory with TFET structure at OFF state (left) and ON state (right).

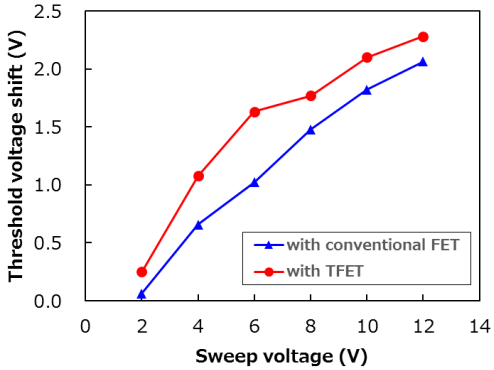

Fig. 8. Relationships between gate sweep voltages and threshold voltage shift.