Extended Abstracts of the 2017 International Conference on Solid State Devices and Materials, Sendai, 2017, pp795-796

Poly-Ge Tri-gate Nanowire Junctionless Charge-Trapping Flash Devices Formed with Low-Temperature Processes for 3D Memory Applications

Yu-Chin Lu[1], Kuei-Shu Chang-Liao[1], Hsin-Kai Fang[1], Kuan-Yi Li[1], Wen-Hsien Huang[2], Chang-Hong Shen[2] and Jia-Min Shieh[2]

[1] National Tsing Hua University
No. 101, Section 2, Kuang-Fu Road, Hsinchu, Taiwan 30013, R.O.C.
Phone: +886-3-5742674, E-mail: lkschang@ess.nthu.edu.tw
[2] National Nano Device Laboratories
No.26, Prosperity Road I, Hsinchu Science Park, Hsinchu, Taiwan 30078, R.O.C.

Abstract

Operation characteristics of polycrystalline germanium (poly-Ge) tri-gate nanowire (NW) junctionless (JL) charge-trapping (CT) flash memory devices fabricated with low-temperature processes were studied in this work. The poly-Ge NW JL flash device shows fast programming and erasing speeds owing to the enhanced electric field in the tunneling oxide. Good retention and endurance properties are also achieved. Therefore, poly-Ge NW JL flash device is promising for high-density three-dimensional (3D) memory applications.

1. Introduction

Polycrystalline germanium (poly-Ge) JL MOSFET device was reported to present good electrical characteristics such as high on/off current ratio (Ion/Ioff) and small subthreshold swing (S.S.) [1]. The implantation and activation processes are not required for poly-Ge JL device because the vacancy and interstitial in poly-Ge film can act as acceptors, which turn the film into p-type [1]. Thus, the fabrication temperature and complexity of poly-Ge JL device are lower than those of poly-Si one. Moreover, the operation speeds of flash memory device are improved by incorporating Ge into Si channel. SiGe buried layers were formed on poly-Si [2] channels in flash memory devices, which show faster operation speeds owing to more carrier supply and enhanced electric field in the tunneling oxide layer.

Recently, laser anneal crystallization (LAC) was applied on poly-crystalline devices [3]. LAC has the advantages of short annealing time and less process thermal budget when compared with other methods [4],[5]. Nevertheless, poor surface morphology was observed at upper poly-Ge film after the LAC process [6]. The aforementioned problem can be effectively resolved by forming nanowire (NW) channel. Moreover, NW channel is specially suitable for JL configuration because JL device is operated by body conduction and depletion. However, the study of poly-Ge flash memory device is rarely seen. In this work, operation characteristics of poly-Ge JL charge-trapping (CT) flash memory device with tri-gate NW channel were studied. All fabrication processes of poly-Ge flash device were performed below 475°C. Planar capacitor device was also fabricated and compared to investigate the electric-field in the tunneling oxide enhanced by using tri-gate NW channel.

2. Devices Fabrication

Both poly-Ge NW JL and planar capacitor flash devices were fabricated on 6-inch Si wafers. A 200-nm thick SiO_2 and a 50-nm thick Si_3N_4 buried layer were sequentially deposited. A 100-nm thick poly-Ge film was deposited by an inductively coupled plasma chemical vapor deposition (ICPCVD) system. Then, a Nd:YAG green nanosecond spike laser annealing was performed increase the grain size. The undoped poly-Ge film was naturally p-type with a concentration of ~10^{18} cm^{-3} measured by Hall method. After poly-Ge thin film was formed on NW JL and planar capacitor samples, one was sent to form the body region of planar capacitor device by using I-line lithography and reactive ion etching (RIE) processes. The other one was sent to form the active region of NW channel device and the process is similar as in [3]. Next, dielectrics in gate stacks for NW JL and planar capacitor samples were the same, and they were deposited by an atomic layer deposition (ALD) system. First, a thin GeO_2 buffer tunneling layer was grown on the surface of poly-Ge by an H_2O plasma treatment. Then, a 3-nm thick Al_2O_3 tunneling layer, an HfO_2 (3.5 nm)/HfAlO (4.5 nm) bandgap-engineered stack-trapping layer, and a 15-nm thick Al_2O_3 blocking layer were sequentially deposited by ALD. Afterwards, TiN metal gate was deposited by a physical vapor deposition (PVD) system. Gate and capacitor regions were defined and transferred. Standard passivation and metallization processes were performed. Then a sintering was carried out to complete the fabrication for both devices.

3. Results and discussions

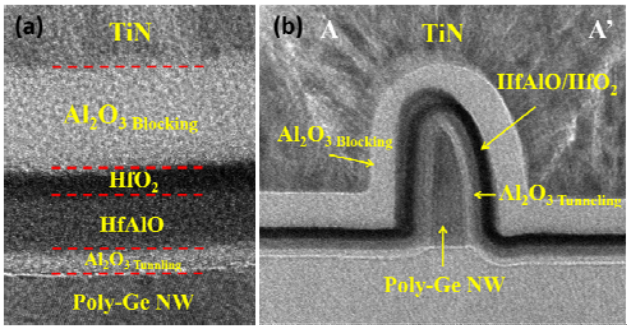

Fig. 1. Cross-sectional TEM images of poly-Ge (a) planar capacitor and (b) NW JL flash devices.

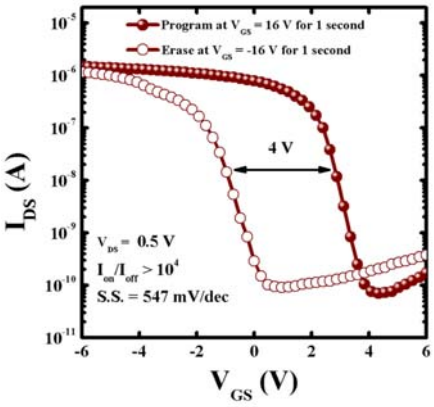

Fig. 2. I_{DS} versus V_{GS} of poly-Ge NW JL flash device.

Fig. 1 shows transmission electron microscopy (TEM) images of poly-Ge (a) capacitor and (b) NW JL flash devices with HfO_2/HfAlO trapping layers. The dielectrics in gate stack are uniformly deposited as shown in Fig. 1(a). In Fig. 1(b), poly-Ge NW JL channel with a width of 13 nm and a height of 30 nm is clearly observed. Fig. 2 shows drain current (I_{DS}) versus gate voltages (V_{GS}) characteristics of poly-Ge NW JL flash device at drain voltage (V_{DS}) = 0.5 V. The I_{on}/I_{off} ratio is larger than 10^4, which is comparable or better than that of crystalline Ge device [8]. The high I_{on}/I_{off} ratio can be due to the small width of NW, by which the poly-Ge JL channel can be effectively depleted.

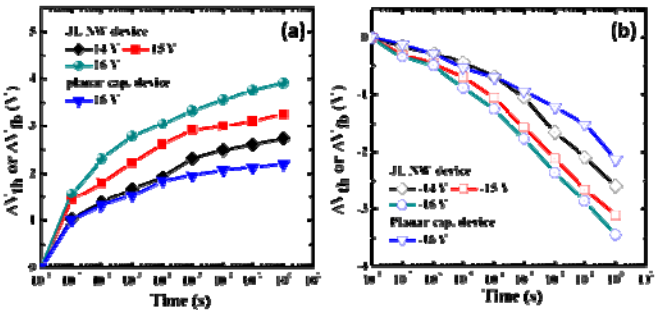

Fig. 3. Operation speeds of poly-Ge NW JL and planar capacitor flash devices: (a) programming speed (b) erasing speed.

Fig. 3(a) shows the programming speeds of poly-Ge NW JL flash devices and planar capacitor flash device at V_{GS} of 14~16 V and 16 V, respectively. Device with NW JL channel shows much faster programming speed and larger memory window than planar capacitor one even when a smaller V_{GS} is applied. Fig. 3(b) shows erasing speeds of poly-Ge NW JL and planar capacitor flash devices. Devices were programmed at the V_{GS} values in Fig. 3(a) for 1 s before erasing speed measurements. The ΔV_{th} and ΔV_{fb} refer to V_{th} in NW JL and V_{fb} in planar capacitor devices of program state, respectively. The erasing speed of NW JL device is faster than that of planar one due to enhanced electric field in the tunneling oxide.

Fig. 4(a) shows retention characteristics of poly-Ge NW JL and planar capacitor flash devices. Both devices were programmed for a memory window of 2 V and tested at room temperature and 85°C, respectively. The retention performance of NW JL device is similar to that of planar capacitor one, suggesting that the charge loss is not influenced by the curvature of NW channel. The endurance characteristics of poly-Ge NW JL and planar capacitor flash devices are shown in Fig. 4(b). Poly-Ge NW JL flash device keeps a larger memory window of ~2 V after 10^4 P/E cycles while planar capacitor one fails after 100 cycles. The better endurance performance of NW JL device may be attributed to the reduced grain boundaries in poly-Ge film by its NW configuration.

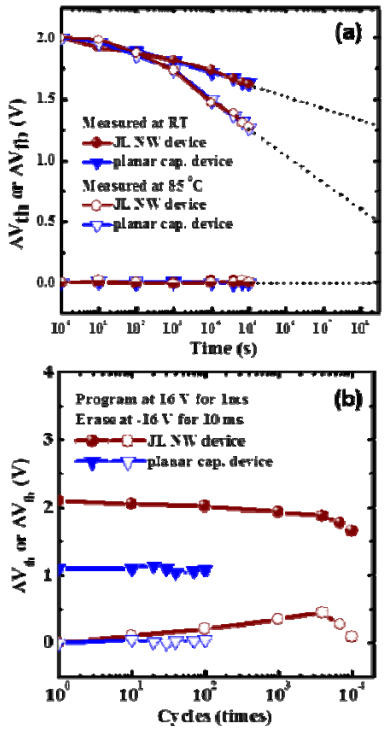

Fig. 4. (a) Retention and (b) endurance characteristics of poly-Ge NW JL and planar capacitor flash devices.

4. Conclusions

Operation characteristics of poly-Ge NW JL and planar capacitor flash devices formed with low-temperature processes were investigated. Fast operation speeds, good retention and endurance performances were achieved by device with NW JL. Thus, poly-Ge NW JL flash devices formed with low temperature processes are promising for high-density 3D memory applications.

References

[1] Y. Kamata et al., *VLSI Symp. Tech. Dig.*, Jun. 2013, pp. 94-95.

[2] C.-Y. Chen et al., *IEEE Electron Device Lett.* 35 (2014) 1025-1027.

[3] C.-C. Yang et al., *IEDM Tech. Dig.* (2014) 16.3.1- 16.3.4.

[4] T. Sadoh et al., *Applied Physics Letters*. 89 (2006) 192114.

[5] J.-H. Park et al., *Applied Physics Letters*. 91, (2007) 143107.

[6] W.-H. Huang et al., *Applied Physics Letters*. 108 (2016) 243502.

[7] C.-W. Chen et al., *IEEE Trans. Electron Devices*. 61, (2014) 2656-2661.

[8] T.-H. Hsu et al., *IEDM Tech. Dig.* (2007) 913-916.