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A 2.4 – 3.2 GHz Robust Self-Injecting Injection-Locked PLL

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***Abstract*—This paper proposes a robust self-injecting injection-locked phase locked loop (SI-ILPLL). A sub-sampling phase detector based phase alignment loop is used to self-align the phase between the injection pulse and the voltage-controlled oscillator (VCO) output. A novel phase frequency detector with adaptive loop selector is proposed to switch the frequency locking loop and phase alignment loop adaptively by checking phase error. The pulse generator can self-inject pulse to VCO for injection locking. The SI-ILPLL performs the injection locking autonomously and shows excellent robustness to environmental interferences. It can self-recover the lock quickly after the disturbance disappears. The SI-ILPLL is implemented in 65 nm CMOS technology. The measured root-means-square (RMS) jitter is 131fs at output frequency of 3.2 GHz. The power consumption is 7.4 mW under 1.2 V supply voltage. It achieves a figure of merit (FoM) of -249 dB.**

1. Introduction

Injection locked technique has been demonstrated a promising method to generate high frequency clocks with very low jitter [1]-[5]. For the injection-locked PLL (ILPLL), the injection timing needs careful adjustment in order to achieve good jitter reduction effect.

Previous ILPLLs with manually [3] and adaptive injection timing alignment [4][5] both need complicated external control and strict operating orders, in order to implement the injection locking. Consequently, once these ILPLLs are unlocked by intense supply interference, they will not be able to self-regain injection locking. In another word, they are susceptible to supply interferences.

This paper proposes a robust self-injecting injection-locked phase locked loop (SI-ILPLL). A novel phase frequency detector with adaptive loop selector (ALS-PFD) is proposed to switch the frequency locking loop (FLL) and phase alignment loop (PAL) adaptively by checking phase error. The pulse generator (PG) can self-inject pulse to VCO for injection locked. Compared with previous ILPLLs, the SI-ILPLL performs the injection locking autonomously. Therefore, the SI-ILPLL shows excellent robustness to environmental disturbances. If it is unlocked by intense environmental disturbances, it can self-recover the injection locking quickly after the disturbance disappears.

2. Robust operation analysis and circuits design

Fig. 1 shows the architecture of the proposed SI-ILPLL. It consists of an injection locked VCO, a differential loop filter (LPF), an auxiliary FLL and a PAL. The SI-ILPLL works as follows. The FLL loop starts to bring the ILVCO to the target frequency. When the ALS-PFD judges that the phase error is small enough, FLL is disconnected from the loop and PAL is enabled and continues to align the phase between the VCO output and the reference clock. The PG is also enabled to inject pulse to the VCO simultaneously during the PAL process.

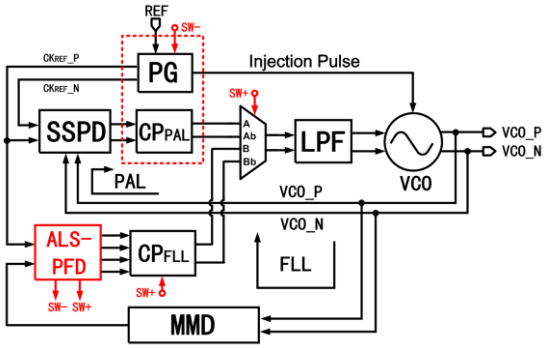
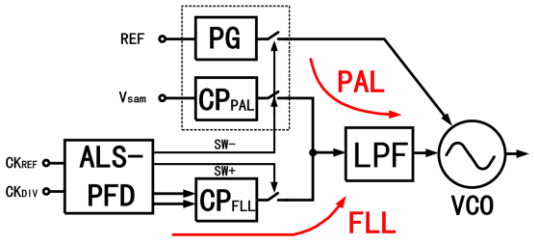


Fig. 1. Block diagram of proposed SI-ILPLL.

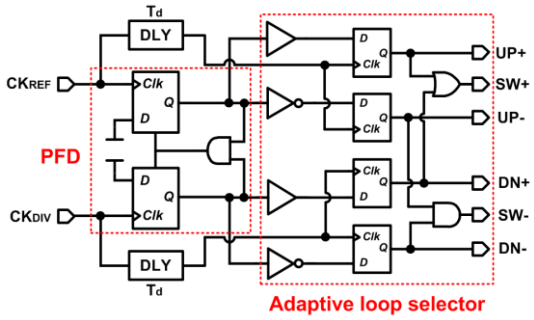
Previous ILPLLs must follow complicated strict operating procedures, which are controlled by off-chip signals, in order to achieve injection locking [1]-[5]. However, with the help of ALS-PFD, the PAL and PG in the proposed SI-ILPLL can operate simultaneously for self-phase-alignment and self-injecting. The ALS-PFD adaptively selects the operating loop of the SI-ILPLL, and PG can self-inject pulse to the VCO for injection locked. Thus, the whole frequency locking, phase alignment and injection locking process can operate autonomously. It obviates traditional external signals that are used to control the operating states of ILPLL. If the SI-ILPLL loses locking due to environmental interferences, the ALS-PFD block will re-enable FLL loop and restart the locking process. It can regain injection locking quickly after the disturbance disappears. Therefore, the proposed SI-ILPLL is robust to environmental interferences.

Fig. 2 (a) illustrates the detailed schematic of the locking procedure of FLL and PAL and Fig. 2 (b) shows the circuit implementation of the ALS-PFD. In addition to output phase detection signal (UP+/UP- and DN+/DN-), ALS-PFD generates two control signals “SW+” and “SW-” to adaptively select the operating loops of the SI-ILPLL based on the phase error.

When the phase error between the CK_{REF} and CK_{DIV} is larger than T_d, SI-ILPLL operates at the frequency locking mode. SW+ is set high and SW- is set low, FLL is enabled to dominate the locking process, and PAL is switched off. When the phase error is smaller than T_d, it means that the phase error falls into the locking range of the PAL and PG. So SW- is set high and SW+ is set low by the ALS-PFD. The PAL is chosen to lead the phase alignment process and the PG is also enabled to self-inject pulse to the VCO. At the same time, FLL is disconnected from the loop and CP_{FLL} is turned off to save power. T_d in this design is set to be 2 ns. Therefore the operating mode of SI-ILPLL can be selected adaptively with the help of ALS-PFD and thus the SI-ILPLL can be injection locked autonomously, without any assistance of external state control signal.



(a)



(b)

Fig. 2. (a) Detailed schematic of the locking procedure of FLL and PAL, (b) circuit implementation of the ALS-PFD.

3. Measurement results

The proposed SI-ILPLL is fabricated in a 65 nm CMOS process with an active area of 1 x 0.7 mm^2. Fig. 3 (a) shows the die photograph of the chip and Fig. 3(b) presents the measured phase noise. When operating at a frequency of 3.2 GHz, the RMS jitter integrated from 1 kHz to 30 MHz is 131 fs with injection locked. Power consumption is 7.4 mW.

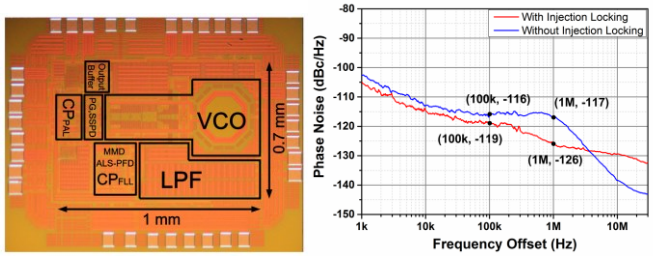


Fig. 3. (a) Die photograph, (b) measured phase noise of the SI-ILPLL.

Fig. 4 shows the measured frequency transient responses under interference of the proposed SI-ILPLL and ILPLL in [4] respectively. When added with a periodic pulse to the VCO supply as disturbance, the proposed SI-ILPLL loses lock but self-regains locked in about 7 µs after the disturbance disappears. While the ILPLL in [4] lost its lock immediately after the disturbance showed up and could not self-regain the lock even when the disturbance disappeared.

Table I summarize the performance of this work.

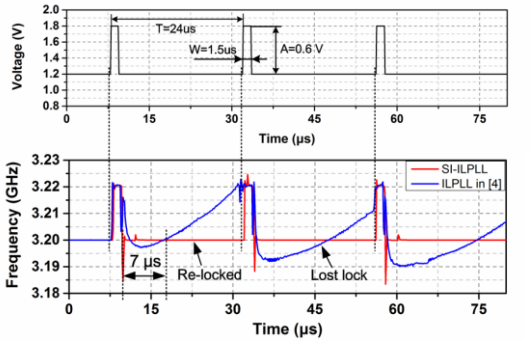


Fig. 4. Measured frequency transient responses when disturbances is added to the VCO supply of the proposed SI-ILPLL and ILPLL in [4], respectively.

Table I Performance summary and comparison

	This work	[3]	[4]	[5]
Technology	**65nm**	65nm	65nm	40nm
Freq. [GHz]	**2.4 – 3.2**	2.8 – 3.2	2.4 – 3.6	2.25–2.7
Ref.[MHz]	**200**	120	400	150
Power [mW]	**7.4@3.2GHz**	4.6@3GHz	9.1@3GHz	3.2@2.25GHz
Area [mm^2]	**0.7**	0.12	0.6	0.01
RMS jitter [fs] (range)	**131 [1k~30M]**	142 [10k~40M]	146 [1k~30M]	1280 [10k~100M]
FoM [dB][a]	**-249**	-250	-247	-233
Calibration method	**Self-Aligned**	Manually	Self-Aligned	Self-Aligned
Interference robustness	**Yes**	No	No	No

[a] $\text{FoM} = 20\log\left(\frac{\sigma_t}{1s}\right) + 10\log\left(\frac{P}{1mW}\right)$.

4. Conclusions

This paper proposed a robust SI-ILPLL. A novel ALS-PFD was proposed to switch the frequency locking loop and phase alignment loop adaptively and dynamically based on the phase error. Compared with previous ILPLLs, the SI-ILPLL was robust to environmental interferences. The SI-ILPLL achieved a FoM of -249 dB.

Acknowledgment

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