PS-5-08

Low power UWB CMOS LNA using Resistive Feedback and Current-Reused Techniques

Jyh-Chyurn Guo and Ching-Shiang Lin
Institute of Electronics Engineering, National Chiao Tung University, Hsinchu, Taiwan
Tel: +886-3-5131368, Fax: +886-3-5724361, E-mail: jcguo@mail.nctu.edu.tw

Abstract

A ultra-wideband (UWB) low noise amplifier (LNA) was designed and fabricated in 0.18μm CMOS technology. The successful integration of current-reused and forward body biasing (FBB) techniques in a cascade amplifier can enable an aggressive scaling of the supply voltages, V_{DD} and V_{G1} to 1.0V and 0.53V. The low voltage feature from FBB leads to more than 50% saving of power dissipation to 5.2mW. The measured power gain (S_{21}) can reach 10.55~12.6dB and noise figure (NF_{50}) is 3.2~3.95 dB through the UWB (3~10.5GHz). This UWB LNA with small chip area (0.69mm^2) provides a solution of low voltages, low power, and low cost.

I. Introduction

The ultra-wideband (UWB) transceivers with stringent requirements of high data rate and low power in short range communication create a valuable application area to exploring RF CMOS technology. For UWB receiver front-end circuits, LNA design faces critical challenges due to FCC's stringent power-emission limitation at the transmitter and additional transmission path loss. Among the well known solutions, distributed amplifier (DA) can provide wideband input matching and flat gain, but high power consumption and large chip area have been the problems when used in UWB system [1]-[2]. RC feedback topology is a viable option, attributed to acceptable wideband matching and gain flatness. Unfortunately, it cannot meet the requirement of high gain and low noise figure at low power [3]. Common gate (CG) may save chip area, due to simple circuit topology for broadband input matching, but high power dissipation for sufficient gain remains a bottleneck [4]. Current-reused technique combined with resistive feedback becomes a promising solution for gain boost through UWB but high power dissipation again becomes the major concern [5]-[6]. Therefore, low power design appears as the most stringent challenge to UWB LNA aimed at hand-held wireless applications. In this paper, a UWB LNA with successful integration of resistive feedback, current-reused, and forward body biasing (FBB) techniques can realize wideband input matching, flat gain, low noise, and most importantly low power dissipation from low voltage, using low cost 0.18μm CMOS technology.

II. UWB LNA Circuit design and analysis

A. UWB LNA Circuit Topology

Fig.1 illustrates the circuit schematics of the proposed UWB LNA, which is a two-stage cascade topology incorporating resistive feedback (R_{fb} and C_{fb}) for wideband input matching, current-reused technique with inter-stage series LC (L_{g2}, C_{gs2}, L_{s2}, and C_{g2}) for gain boost, without increase of dc power dissipation (P_{DC}), inductive shunt peaking (L_{d2}) at output stage for bandwidth extension, and FBB scheme for further power reduction from lower voltage. The operational principle of this two-stage cascade amplifier is described as follows. First, for the resistive feedback, the wide band input matching is achieved by generating two notch points in the input return loss, S_{11} corresponding to two poles of resonance frequencies, one determined by inductive source degeneration (L_{g1}, L_{s1}, and C_{gs1}) at the input stage and the other by a series LC (L_{g2}, C_{gs2}, L_{s2}, and C_{g2}) through R_{fb} and C_{fb} at the inter-stage. Secondly, the inter-stage series LC can realize gain boost through ac current amplification, without increase of P_{DC}, namely current-reused method. Finally, FBB (V_{BS}=0.5~0.6V) was adopted to further reduce the P_{DC} attributed to lower dc voltages (V_{DD} and V_{G1}). In the following, detailed circuit topology analysis will be performed according to aforementioned three aspects.

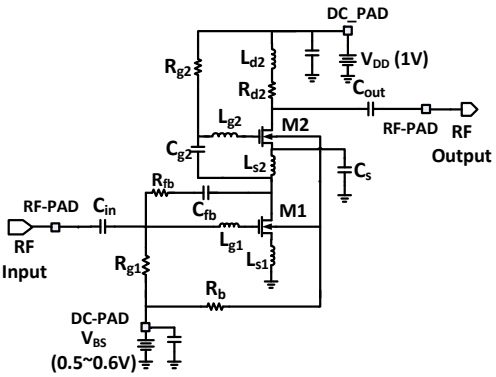

Fig. 1 The circuit schematics of the UWB LNA as a two-stage cascade amplifier consisting of resistive feedback at input stage, series LC at inter-stage, inductive shunt peaking at output stage.

B. Current-reused Method for Gain Boost

As shown in Fig. 2(a) and (b), a comparison between the typical cascode amplifier and cascade amplifier adopting inter-stage series LC, can facilitate analysis of the operational principle and current-reused method for gain boost. The ac current gain can be derived, given as $|i_{d2}/i_{d1}|_{max}=|i_{d2}/i_{d1}|_{\omega=\omega 02}=\omega_{T2}/\omega_{02}$ ($\omega_{T2}=g_{m2}/C_{gs2}$, $\omega_{02}=[(1+C_{gs2}/C_{g2})/L_{g2}C_{gs2}]^{1/2}$), $\omega_{T2} >> \omega_{02}$ and $|i_{d2}/i_{d1}|_{max} >>1$.

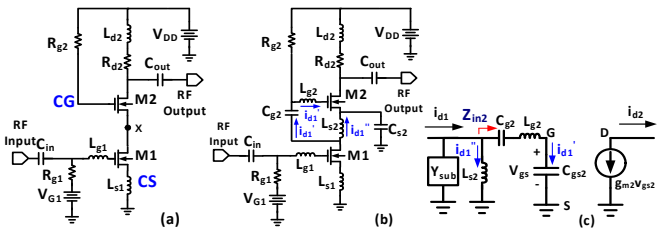

Fig.2 (a) Cascode amplifier (b) cascade amplifier with inter-stage series LC (c) small signal equivalent circuit of (b)

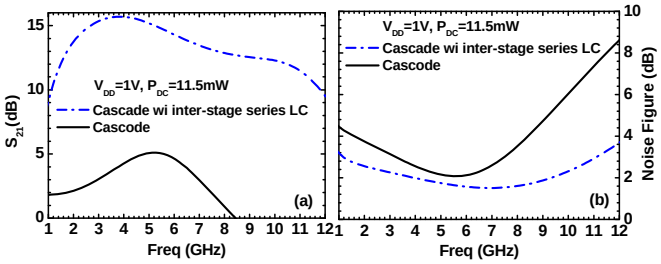

Fig. 3 Comparison of cascode and cascade amplifier with inter-stage series LC (a) power gain S_{21} (b) noise figure, at V_{DD}=1.0V and P_{DC}= 11.5mW.

Fig.3(a) makes a comparison of the power gain S_{21} by ADS simulation at very low V_{DD} to 1.0V and P_{DC}=11.5mW. The cascode amplifier reveals poor power gain, such as $S_{21} \leqq 5.1$dB in narrow band. In contrast, the cascade amplifier adopting inter-stage series LC can offer S_{21} >10dB through very wide band and peak S_{21} up to

15.7 dB. It proves that current reused method can increase power gain S_{21} by around 3.1 times due to ac current gain boost. Fig.3(b) shows that the cascade amplifier with inter-stage series LC can yield lower noise associated with higher S_{21}. Note that the above verification is done at narrow band input matching with minimum S_{11} close to 6GHz (not shown). In the following, resistive feedback will be used for wide band input matching to achieve better gain flatness through UWB. Also, FBB will be applied to push the P_{DC} below 5.5mW, i.e. more than 50% reduction from 11.5mW.

C. Resistive Feedback for Wideband Input Matching

Fig.4(a) illustrates the small signal equivalent circuit of the input stage with resistive feedback for UWB input matching. Herein, $Z_f//Z_{in1}$ results in dual poles resonance at $\omega_{o1,L}$ and $\omega_{o1,H}$, , which determine the bandwidth between $f_L=\omega_{o1,L}/2\pi$ and $f_H=\omega_{o1,H}/2\pi$. As shown in Fig.4(b), the ADS simulation predicts f_L=2.6GHz and f_H=10.5GHz corresponding to Z_f and Z_{in1}, and jointly two minima of mag(S_{11}) at 3.9GHz and 10.2GHz resulted from $Z_{in}=Z_{in1}//Z_f$. It proves that the resistive feedback can realize wideband input matching and meet the UWB requirement.

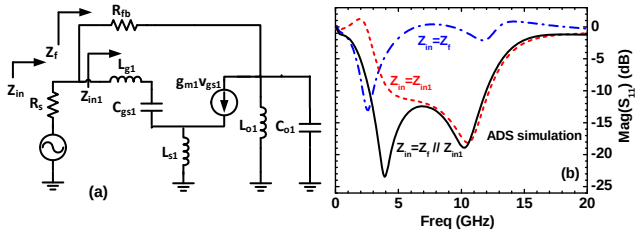

Fig. 4 (a) Equivalent circuit of the input stage with resistive feedback for input matching (b) Mag(S_{11}) at $Z_{in}=Z_f$, Z_{in1}, and $Z_f//Z_{in1}$ by ADS simulation

D. FBB for Further Power Reduction

FBB is proposed as an effective solution for further reduction of the P_{DC} at sufficient S_{21}. Referring to Fig. 1, FBB (V_{BS}>0) is applied to the body of M1 and M2. ADS simulation is done at V_{DD}=1.0V and lower V_{G1} to 0.6V so that power dissipation can be pushed to P_{DC}=5.4mW. As shown in Fig.5 (a), the FBB (V_{BS}=0.6V) can offer $S_{21}\geqq$12dB whereas the ZBB (V_{BS}=0) reveals around 2dB lower S_{21}. Also, Fig.5(b) indicates that FBB enabling higher S_{21} can lead to lower noise figure than ZBB. Another verification was made by increasing V_{DD} and V_{G1} for ZBB to raise S_{21} and lower noise figure to matching the performance of FBB. The results indicate that V_{DD}=1.1V and V_{G1}=0.63V are required for ZBB to reach nearly the same S_{21} ad noise figure, but lead to the penalty of around 36.5% higher P_{DC} to 7.37mW.

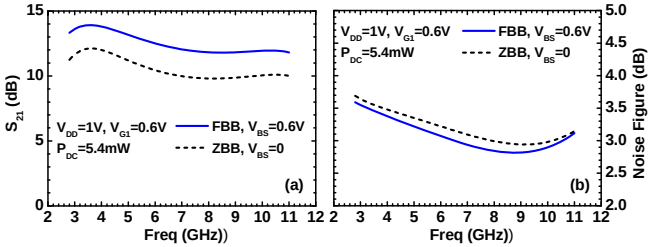

Fig. 5 ADS simulation for UWB LNA at V_{DD}=1.0V, V_{G1}=0.6V, and P_{DC}=5.4mW, different body biases : FBB (V_{BS}=0.6V) and ZBB (V_{BS}=0) (a) power gain S_{21} (b) noise figure.

III. Results and Discussion

The designed UWB LNA was fabricated in 0.18µm RF CMOS technology with small chip area of 0.69 mm^2 including all RF GSG and dc pads. Fig.6(a)~(d) present a comparison of UWB LNA performance parameters (S_{11}, S_{22}, S_{21}, and NF_{50}) from measurement and ADS simulation at fixed V_{DD}=1.0V and minor differences in FBB and power dissipation, such as $V_{G1}=V_{BS}$=0.53V, P_{DC}=5.2mW and $V_{G1}=V_{BS}$=0.6V, P_{DC}=5.4mW, respectively. First, as shown in Fig.6(a) and (b), the measured S_{11} and S_{22} (symbols) can keep below -10dB and -15dB in 3~10.5GHz, but there is some degradation compared to the simulation (lines). As for the power gain and noise figure shown in Fig.6(c) and (d), the measured S_{21} can keep above 10.5dB and NF_{50} is below 3.95dB through UWB, which indicate 0.6~1.7dB lower S_{21} and 0.3~0.6dB higher NF_{50} than the simulation. Table 1 demonstrates performance benchmark on recently published UWB LNA using current-reused technique combined with various circuit topologies, in 0.18µm, 0.13µm, and 90nm CMOS processes [5]-[8]. The comparison indicates that our UWB CMOS LNA can offer some obvious advantages, such as the lowest V_{DD} and power dissipation (P_{DC}=5.2mW), attributed to FBB method, and the lower cost due to small chip size in 0.18µm CMOS technology. According to the specified figure-of-merit FOM=(S_{21}×BW)/(NF_{50}×$P_{DC(mW)}$), the UWB LNA in this paper can offer the best FOM with major contribution from the higher S_{21} at the lowest P_{DC}.

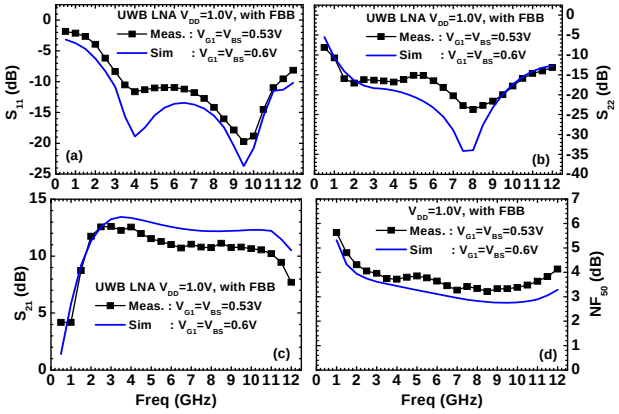

Fig.6 UWB LNA performance by measurement ($V_{G1}=V_{BS}$=0.53V, P_{DC}=5.2mW) and simulation ($V_{G1}=V_{BS}$=0.6V, P_{DC}=5.4mW) at V_{DD}=1.0V (a) S_{11} (b) S_{22} (c) S_{21} ((d) NF_{50}.

Table 1 UWB LNA Performance Benchmark

UWB LNA	This work	[5]	[7]	[6]	[8]
CMOS	0.18µm	0.18µm	0.18µm	0.13µm	90nm
BW(GHz)	3.1~10.6	3.1~10.6	3.1~10.6	3.1~10.6	2.6~10.2
V_{DD}(V)	**1.0**	1.8	1.5	1.8	1.2
V_{BS}(V)	**0.53**	---	---	---	---
P_{DC} (mW)	**5.2**	10.68	4.5 (core)	14.4	7.2
S_{21} (dB)	12.61/10.55	8.15/7.69	12/**5**	12/11	12.5/8.5
NF_{50} (dB)	3.21/3.95	2.5/4.56	5.27/7	2.7/3.7	3/7
S_{11} (dB)	< -10.54	< -17.5	< -13.5	< -7.3	< -9
S_{22} (dB)	< -15.94	< -14.4	< -10.1	< -14	----
S_{12} (dB)	< -27.36	< -39	< -43	< -38.9	< -45
IIP3(dBm)	-2.3	-4	-2.23	-3.8	----
Chip size	0.69	0.435	1.03	0.031(core)	0.64
FOM	**6.474**	2.198	2.78 (core)	2.723	2.771

IV. Conclusion

The UWB LNA in this design presents the advantages of low power dissipation (P_{DC}=5.2mW) from low voltages, such as V_{DD}=1.0V and V_{G1}=0.53V, sufficiently high power gain and low noise (S_{21}=10.55~12.6dB, NF_{50}=3.2~3.95dB) with good flatness through UWB, and small chip area (0.69 mm^2). The integration of current-reused and FBB techniques has been proven as the major factor to realize very low V_{DD} in the cascade amplifier. It provides a promising solution for low voltage and low power UWB LNA design using low cost CMOS technology.

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