

Effects of Channel Profile and Source/Drain Resistance on P-type SnO TFTs

Ming-Hung Wu*, Horng-Chih Lin#, and Pei-Wen Li

Department of Electronics Engineering and Institute of Electronics, National Chiao Tung University,
1001 University Road, Hsinchu 30010, Taiwan

Phone: +886-3-571-2121#54193 E-mail: * e780626@gmail.com; # hclin@faculty.nctu.edu.tw

Abstract

In this work, we simulate and analyze the characteristics of tin monoxide (SnO) thin-film transistors (TFTs) fabricated with the film-profile-engineering (FPE) scheme. The fabricated TFT with channel length (L) of 200 nm shows a high on/off current ratio ($>10^5$) and series source/drain resistance of around $14 \text{ M}\Omega\text{-}\mu\text{m}$. The simulation results show that the FPE device is superior to the devices with a uniform channel thickness in term of switching performance optimization.

1. Introduction

Since the inception of tin monoxide (SnO) active layers for *p*-channel TFTs [1], SnO TFTs have attracted considerable attentions because of their great potential for the implementation of high-performance CMOS circuitries. To date, the fabrication of SnO-based TFTs [2-4] have been conducted in various process schemes. Recently we have proposed an exquisite BEOL-compatible method, namely film-profile-engineering (FPE) that utilizes a suspended bridge as a shadow mask and specific deposition techniques, to deposit gate-stacking heterostructures in a TFT with desirable profiles [5]. In this work, we experimentally demonstrated the feasibility of SnO TFTs in our FPE approach and numerically analyzed electrical characteristics of the FPE SnO TFTs using TCAD simulation (ATLAS Silvaco). Effects of R_{SD} and channel film profile on the characteristics of TFTs are also investigated.

2. Device fabrication

Process flow for the fabrication of SnO TFTs in our proposed FPE approach is summarized in Fig. 1. An *n*-type silicon substrate was used as the back gate. Firstly, a 600 nm-thick TEOS sacrificial oxide and a 200 nm-thick poly-Si hard-mask layer were sequentially deposited over the Si substrate using LPCVD. The poly-Si hard-mask layer was then lithographically patterned, followed by a wet etching to remove the underlying sacrificial oxide layer. Thus, a suspending poly-Si hard-mask bridge is resulted. Next, a nominally 20 nm-thick HfO_2 gate-dielectric layer was deposited using ALD at 250°C , followed by the deposition of a SnO channel layer with nominal thickness of 60 nm using DC magnetron sputtering in an O_2/Ar ambient at room temperature (RT). Finally, a 50 nm-thick Ni was evaporated at RT as S/D electrodes. The samples were then subjected to thermal annealing at 300°C for 30 mins in an oxygen ambient in order to improve the crystallinity of the SnO films. After all, the beauty of the proposed fabrication scheme is its simplicity since only one mask is required for the entire device fabrication.

3. Results and discussion

Fig. 2 shows the cross-sectional TEM (CTEM) micrographs of a fabricated SnO TFT in our proposed FPE approach. The simulated structure depicting the region beneath the suspended bridge is also illustrated. Fig. 2(a) shows that a hard-mask bridge is suspended from the Si substrate and underneath the bridge, there indeed appears the stacking layers of Ni/SnO/ HfO_2 . Channel length (L) of the fabricated TFTs, defined as the distance between source and drain electrodes, is approximately 200 nm. Transfer characteristics of the SnO TFTs displayed in the inset of Fig. 3(a) show that the on/off current ratio is greater than 10^5 and subthreshold swing is 230 mV/dec . It is a known fact that for a short-channel TFT, R_{SD} strongly influences the drive current and must be considered in simulation. The extracted R_{SD} value is approximate $14 \text{ M}\Omega$ based on the Campbell's method [6] (Fig. 3(a)). In addition, the intrinsic transconductance (G_m) and field-effect mobility (μ_{FE}) can be calculated simultaneously based on the relations of $I_D' = V_D/R_{Total} - R_{SD}$ and $G_m' = dI_D'/V_G$, where $R_{Total} = V_D/I_D$. The intrinsic μ_{FE} extracted in Fig 3(b) is $\sim 1.0 \text{ cm}^2/\text{Vs}$, which is five-times higher than the extrinsic one. The R_{SD} value adopted in the simulation is $7 \text{ M}\Omega$ for each electrode based on the results shown in Fig. 3. Fig. 4 shows good matching between the experimental I-V characteristics and simulation data. In addition, impacts of R_{SD} on the electrical characteristics of TFTs are obviously seen in Fig. 5, in particular, in the linear region of the output curves. To further understand the superiority of the FPE profile on SnO TFTs, SnO channels with uniform thickness are further considered. Two thicknesses are simulated, namely, Type-I and Type-II, respectively, denoting the channel thickness being equal to the thinnest (central) and thickest (edge) parts of the experimental FPE channel. Fig. 6 compares the simulated transfer and output curves of TFTs with various channel profiles. TFTs with a Type-II channel exhibits the highest current drive, however, at the expense of extremely poor gate controllability with $I_{on}/I_{off} \sim 0$. Fig. 6(b) shows that the FPE SnO TFTs have ON-current obviously higher than Type-I ones do. Numerical simulation on the hole concentration (n_h) in the SnO channel layer clarifies the origins. Fig. 7 compares the simulation data of TFTs with FPE channel and uniform channels at $V_D = -1 \text{ V}$ and $V_G = 0 \text{ V}$. For the Type-II case, it is difficult to deplete abundant n_h present in a thick channel, resulting high leakage and high I_{off} . On the other hand, the FPE case displays much higher n_h than type I in the regions close to the S/D metals, leading to a reduced contact resistance and thus a higher on current.

3. Conclusions

We have employed the simple FPE method to fabricate p-channel SnO TFTs and performed TCAD simulation to analyze the device performance. The fabricated TFT with L of 200 nm shows a high on/off current ratio ($>10^5$) and subthreshold swing of 230 mV/dec. The effects of R_{SD} are explored as well. From the comparisons made between TFTs with various channel profiles, the FPE device is shown to be beneficial for optimizing the switching characteristics of the SnO TFTs.

Acknowledgments - This work was sponsored in part by the Ministry of Science and Technology, Taiwan, under Grant MOST105-2221-E-009-144-MY3 and NCTU-UCB I-RiCE program, under Grant MOST-106-2911-I-009-301, and Research of Excellence Program MOST 106-2633-E-009-001.

References

- [1] Y. Ogo *et al.*, Appl. Phys. Lett. **93** (2008) 032113-1.
- [2] S. Sunamura *et al.*, IEDM Tech Dig., p. 447 (2012).
- [3] C. W. Zhong *et al.*, IEEE EDL. **36** (2015) 1053.
- [4] Y. J. Choi *et al.*, J. Vac. Sci. Technol. B **33** (2015) 041203-1.
- [5] H. C. Lin *et al.*, IEEE EDL. **34** (2013) 1160
- [6] J. P. Campbell *et al.*, IEEE EDL. **32** (2011) 1047.

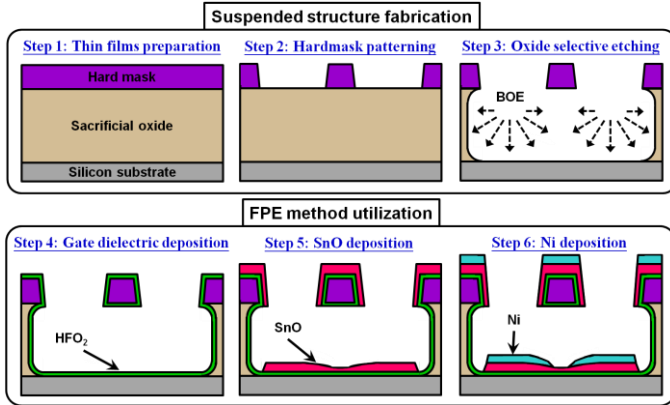


Fig. 1 Process flow for fabricating the p-type SnO TFTs with FPE method.

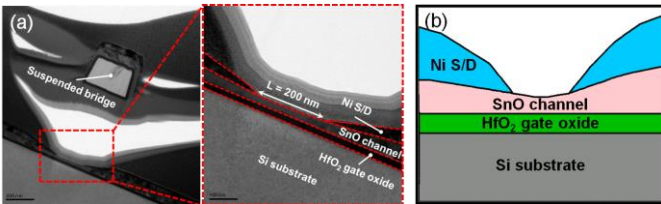


Fig. 2 (a) Cross-sectional TEM images and (b) simulated structure of SnO TFTs with FPE profile.

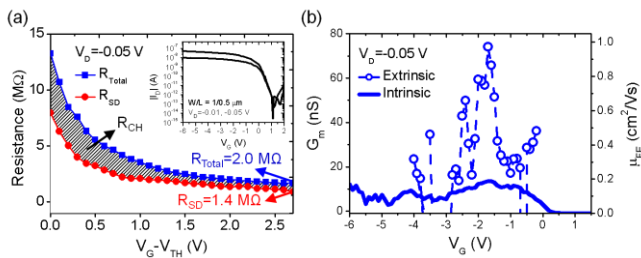


Fig. 3 (a) R_{Total} ($=R_{ch} + R_{SD}$) as a function of gate overdrive and (b)

calculated intrinsic G_m and μ_{FE} as a function of V_G .

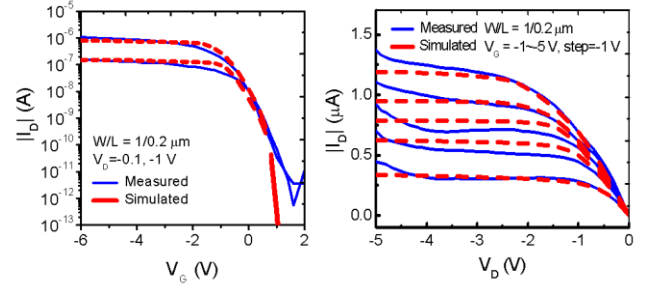


Fig. 4 Measured and simulated transfer and output characteristics of the SnO TFT.

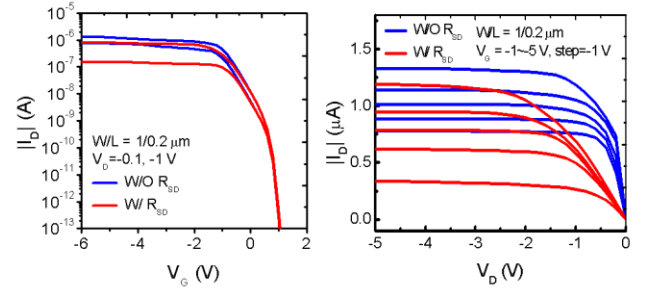


Fig. 5 Simulated transfer and output characteristics of SnO TFTs with and without considering R_{SD} .

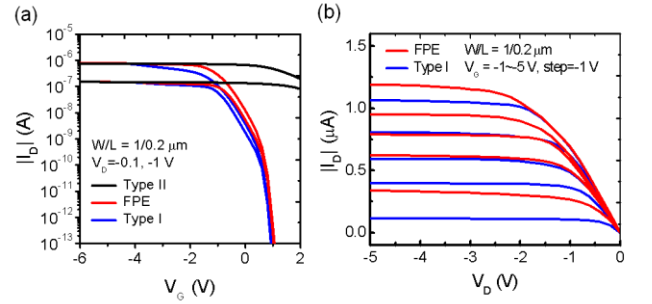


Fig. 6 (a) Simulated transfer characteristics of FPE, type I, and type II devices. (b) Simulated output characteristics of FPE and type I devices.

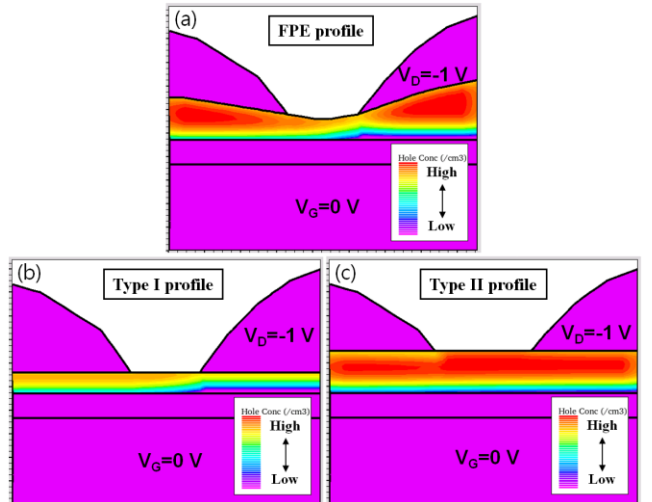


Fig. 7 Simulated n_h in the channel for TFTs of (a) FPE, (b) type I, and (c) type II profile at $V_D = -1$ V and $V_G = 0$ V.