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Nearly ideal spin tunneling efficiency by lowering the trap density at an amorphous-MgO / n^+-Si(001) interface with a SiO_x insertion layer

Mitsuki Ichihara[1], Shoichi Sato[1], Masaaki Tanaka[1,2], and Ryosho Nanake[1,3]

[1]Department of Electrical Engineering and Information Systems, The University of Tokyo,
[2]Center for Spintronics Research Network (CSRN), The University of Tokyo,
[3]Institute for Innovation in International Engineering Education, The University of Tokyo,
7-3-1 Hongo, Bunkyo-ku, Tokyo 113-8656, Japan
Phone: +81-3-5841-6729 Email: ichihara@cryst.t.u-tokyo.ac.jp

Abstract

We achieved nearly ideal spin tunneling efficiency η by lowering the interface trap density D_{it} with a SiO_x layer in Fe / Mg / amorphous-MgO(1.0 – 1.5 nm) / plasma-oxidized SiO_x(~0.2 nm) / n^+-Si(001) junctions. We estimated the tunneling electron spin polarization P_S in Si by narrower three-terminal Hanle signals measured at 4 K. At the optimum MgO thickness and oxidation time, P_S = 41% which is nearly equal to the spin polarization P_{FM} (= 44%) of Fe at the Fermi level, and $\eta = P_S/P_{FM}$ = 0.93. By quantitatively estimating D_{it} and P_S of various junctions, we show that lowering D_{it} is crucial to obtain η ≅ 1.

1. Introduction

To realize Si-based spin-functional devices with a high magneto-current ratio, spin injection/extraction into/from Si through a ferromagnetic metal(FM)/MgO/Si tunnel junction has been extensively studied [1-3]. For such devices, highly-efficient spin injection/extraction is required and it can be measured by spin tunneling efficiency $\eta = P_S/P_{FM}$, where P_S is tunneling electron spin polarization in Si and P_{FM} is the spin polarization of FM at the Fermi level. Although $\eta = 1$ is ideal, the η values reported so far were significantly smaller than 1; η = 0.17 at 8 – 300 K in a Fe/MgO/n^+-Si junction [1] and η = 0.41 at 300 K in a Co_2FeSi/MgO/Si junction [2]. In our previous paper, we found that the spin polarization of electrons passing through a ferromagnetic tunnel junction is reduced by a magnetically-dead layer formed at the FM/MgO interface, and demonstrated that an ultra-thin Mg insertion layer effectively suppresses the magnetic degradation [3]. In such junctions, we obtained η = 0.41 at 4 K, but it is not high enough. On the other hand, since electron trap states at the MgO/Si interface can be spin flip centers, η is possibly improved by lowering the interface trap density D_{it}, although it has not been demonstrated ever. In this study, we show that nearly ideal η = 0.93 is achieved in a Fe/Mg/MgO/Si junction by lowering D_{it} with a plasma oxidation of the MgO/Si structure during the junction formation.

2. Device preparation

The sample preparation was as follows: After thermal cleaning of a H-terminated Si(001) substrate in an ultra-high vacuum, a MgO layer with the thickness d_{MgO} = 1.0, 1.2, and 1.5 nm was deposited at room temperature by electron beam (EB) evaporation. Subsequently, the MgO/Si structure was oxidized at room temperature by a RF plasma source for oxidation time t_{ox} = 1 and 3 min, during which an ultrathin SiO_x layer was formed between MgO and Si. A non-oxidized MgO/Si structure was also prepared, and it is denoted by t_{ox} = 0 min. On this surface, three types of structure were prepared at room temperature: (from top to bottom) (1)For three-terminal Hanle measurements, an Al(10 nm)/Mg (1 nm)/Fe (3 nm)/Mg (1 nm) was deposited on a MgO(d_{MgO} = 1.0, 1.2, and 1.5 nm) layer by molecular beam epitaxy (MBE), (2)For *C*-*V* measurements and the conductance method with MOS capacitors[4], an Al(10 nm)/MgO (4 nm) was deposited on a MgO(d_{MgO} = 1.2 nm) layer by EB evaporation and MBE, and (3)For X-ray photoelectron spectroscopy (XPS) measurements, a 3-nm-thick Al was deposited on a MgO(d_{MgO} = 1.0 nm) layer by MBE. After exposure to air, the fabrication process of the top and bottom electrodes for (1) and (2) was the same as that in the previous paper [3]. Phosphorus-doped Si(001) substrates with ~1 mΩcm and ~100 mΩcm were used for (1)(3) and (2), respectively. The diameter of a circular pillar junction for (1) was 17.8 μm, whereas that for (2) was 178 μm. Figure 1 shows a three-terminal device structure with the junction structure (1) and the three-terminal Hanle measurement setup, in which the voltage change ΔV^N is measured with a constant negative current I_B (spin extraction geometry) driven from the top to the bottom electrodes while a perpendicular magnetic field is swept from -3 to 3 kOe.

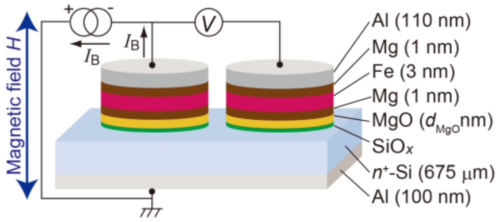

Fig. 1 Schematic structure of a device with multi-layered magnetic junctions and the three-terminal Hanle measurement set up.

3. Characterization of SiO_x formation

From XPS spectra of Si 2*p* in Fig. 2(a), the sample with d_{MgO} = 1.0 nm and t_{ox} = 0 min does not have SiO_x, whereas the sample with d_{MgO} = 1.0 nm and t_{ox} = 1 min has a SiO_x layer with x ~ 2. By the angle-resolved XPS spectrum of Si 2p, the thickness of SiO_x d_{SiOx} was estimated to be 0.26 nm. Figure 2(b) shows resistance-area product RA at zero bias of all the three-terminal samples, which were estimated from the I-V curves measured at 4 K. For the same d_{MgO}, RA increases exponentially with increasing t_{ox}, indicating that d_{SiOx} increases with increasing t_{ox}.

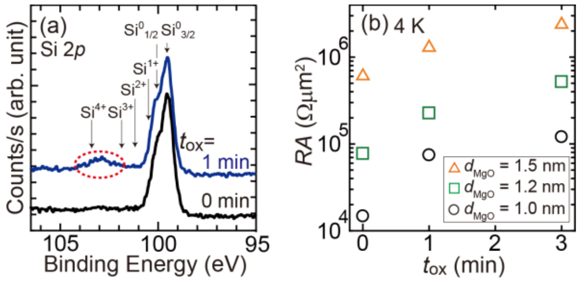

Fig. 2 (a) X-ray photoelectron spectroscopy (XPS) spectra of Si 2p measured, where black and blue curves are the spectra of the Al(3 nm)/MgO(1 nm)/Si (t_{ox} = 0 min) and Al(3 nm)/MgO(1 nm)/SiO_x/Si (t_{ox} = 1 min), respectively. (b) Resistance-area product (RA) at zero bias voltage of the junction plotted as a function of t_{ox}, which were estimated from I-V characteristics measured at 4 K. The open black circles, open green squares, and open orange triangles are the values for MgO thickness d_{MgO} = 1.0, 1.2, and 1.5 nm, respectively.

4. Spin extraction experiments and estimation of η

Figure 3(a) shows Hanle signals ΔV^N of the devices with d_{MgO} = 1.2 nm measured at 4 K with I_B = –30 mA, where black, blue, and red curves are t_{ox}= 0, 1, and 3 min, respectively. We estimated the spin lifetime τ_S and P_S by fitting a theoretical curve [3], which is the light green curve superimposed on each signal. Whereas τ_S was almost the same among the devices, P_S was changed depending on t_{ox}. In the same manner, P_S in all the devices were estimated, and these are plotted as a function of t_{ox} in Fig. 3(b). Interestingly, as t_{ox} increases, P_S (and η) for the devices with d_{MgO} = 1.2 and 1.5 nm increase at first, show the maximum at t_{ox} = 1 min, and then slightly decrease. This behavior

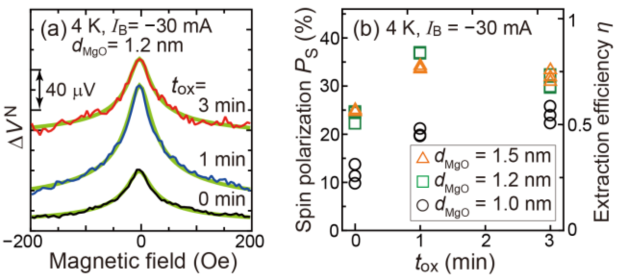

Fig. 3 (a) Narrower three-terminal Hanle signals ΔV^N of devices with d_{MgO} = 1.2 nm measured at 4 K with I_B = –30 mA, where black, blue, and red curves are ΔV^N of the devices with t_{ox} = 0, 1, and 3 min, respectively, and the light green curve superimposed on each ΔV^N is the fitting curve with Eq. (2) in [3]. (b) Tunneling spin polarization P_S in Si and spin tunneling efficiency η plotted as a function of t_{ox}, where each value was estimated from ΔV^N measured at 4 K with I_B = –30 mA. The open black circles, open green squares, and open orange triangles are the values for d_{MgO} = 1.0, 1.2, and 1.5 nm, respectively.

cannot be explained by the RA – t_{ox} relation in Fig. 2(b), in which RA increases with increasing t_{ox}.

We also measured the I_B dependence of P_S of the device with d_{MgO} = 1.2 nm and t_{ox} = 1min, and found that P_S increases with decreasing I_B. At I_B = –15 mA, we obtained the maximum value of P_S = 0.41, which corresponds to η = 0.93.

5. Relation between P_S and interface trap density D_{it}

Figure 4 shows D_{it} estimated from the conductance method at room temperature, where d_{MgO} = 1.2 nm and black, blue, and red circles are t_{ox}= 0, 1, and 3 min, respectively. As t_{ox} increases from t_{ox} = 0 min, D_{it} in whole the energy range decreases at t_{ox} = 1 min, and then it slightly increases at t_{ox} = 3 min. This behavior is highly correlated with the t_{ox} dependence of P_S for d_{MgO} = 1.2 nm in Fig. 3(b); the device with lower D_{it} shows higher P_S. Thus, we concluded that the highest P_S = 41% (η = 0.93) in this study is achieved by lowering D_{it} at the insulator/Si interface.

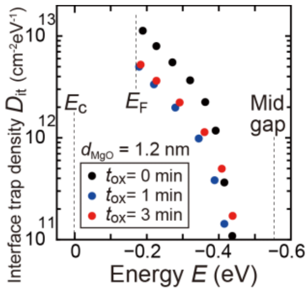

Fig. 4 Interface trap density D_{it} in capacitors with d_{MgO} = 1.2 nm and t_{ox} = 0, 1, and 3 min plotted by electron energy E, where the origin of E is set at the conduction band edge E_c of Si, the middle of the bandgap of Si is indicated by "Mid gap", and E_F denotes the Fermi level of the Si substrate. The black, blue, and red circles are D_{it} in the capacitors with t_{ox} = 0, 1, and 3 min, respectively.

6. Conclusion

We have achieved the spin tunneling efficiency η = P_S/P_{FM} value of 0.93, which is the highest ever reported by lowering D_{it} at the insulator/Si interface with the SiO_x (x ~2) insertion layer. The η obtained in this study is nearly ideal in the junctions using an amorphous insulator layer, *i.e*, without the spin filter effect.

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