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Room temperature high peak-to-valley current ratio of CaF_2/Si triple-barrier resonant-tunneling diode grown on Si

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Abstract

Room temperature Negative Differential Resistance (NDR) with peak-to-valley current ratio (PVCR) as high as 10^5 and with peak current density (J_{peak}) larger than 100 kA/cm^2 has been demonstrated using atomically-thin-CaF_2 energy barrier layers and Si quantum-wells triple-barrier resonant tunneling diode (RTD) structures. NDR characteristics were reasonably explained using theoretical analysis using simple model based on Esaki-Tsu formula and transfer matrix method.

1. Introduction

The dimensions of the elements comprising integrated circuits have been decreasing to the nanoscale. One essential building block for nanoscale solid-state devices is electric potential sequences for realizing electronic functions such as electron injection, transport, and storage, which can be implemented using the energy band discontinuity at atomically abrupt heterointerfaces. A CaF_2/Si heterostructure is an attractive candidate for application to Si-based integrated devices, such as resonant-tunneling diodes (RTDs)[1,2] and transistor, coulomb blockade devices, resistance switching devices [3] because of the large conduction band discontinuity (ΔE_C~2.3 eV)[4,5] at the heterointerface and the small lattice mismatch with silicon owing to the similar cubic-based crystalline structures. Owing to the large ΔE_C and energy band gap (E_g for CaF_2 is 12.1 eV[6,7]), the leakage current is expected to be suppressed to a low level even at room temperature (RT) and, moreover, the voltage for tunneling transport can be controlled by utilizing a multiple-quantum-well tunneling scheme, such as resonant tunneling with appropriately designed quantum-well (QW) layer thickness sequences. In this study, we have demonstrated room temperature NDR characteristics with high-PVCR using CaF_2/Si/CaF_2/Si/CaF_2 triple-barrier RTD structure simultaneously exhibiting high peak current density.

2. Experiment

CaF_2 and Si have similar crystalline structure and the misfit is +0.6 % at RT, which enables multilayered epitaxial growth on Si substrate. Figure 1 shows the schematic device structure and band diagram (flat band) used in this study. The device comprises a CaF_2/Si/CaF_2/Si/CaF_2 triple-barrier resonant-tunneling (TBRTD) structure grown on Si substrate. The CaF_2 layers act as energy barriers for resonant-tunneling through Si-QWs, which act as energy filter of injected electrons. The upper n-type As-doped n-type Si layer was used as a collector of electrons passing through RTD structure and n-type Si substrate is used as an electron emitter in this study.

An 30-nm-thick SiO_2 layer was formed by wet oxidation on a n-type Si(111) substrate with a 0.1° off miscut angle and a resistivity of less than 4 mΩ·cm. Subsequently, 2-μm-diameter holes were formed by photolithography and wet chemical etching, followed by formation of a protective oxide layer on the Si surface at the bottom of the hole by boiling in a solution of SC2. After loading into an ultra-high-vacuum (UHV) chamber, 0.62-nm-thick-CaF_2/2.5–nm-thick-Si/0.62-nm-thick-CaF_2/1.5-nm-thick-Si/0.62-nm -thick-CaF_2 multilayered structures were grown on the bottom Si by a molecular beam epitaxy (MBE)-based technique[8,9]. Si layers were grown by electron-beam evaporation and CaF_2 layers were grown with a partially ionized CaF_2 beam to obtain an atomically flat layers. The first 0.62-nm-thick CaF_2 layer was grown on Si at T_s = 650°C, followed by Si-QW growth at T_s = 80 °C[10,11]. The thickness of the Si-QW layer significantly affects the voltage for the peak current (V_{peak}), which corresponds to the alignment of the quasi-energy levels in the Si-QWs. Finally, the top 5 nm-thick-Si layer was grown with As flux as an n-type dopant. This resulted in an As atomic density of 10^{19} cm^{-3}. After the growth, *in situ* annealing was carried out at 650 °C for 30 min to improve the crystalline quality by solid phase epitaxy. After unloading from the UHV chamber, 200×200 μm^2 square Au/Al electrode pads were formed by lift-off.

3. Results and discussion

Figure 2 shows I-V curves exhibiting room temperature NDR characteristic of CaF_2/Si TBRTD where inlet shows linear plot. The peak voltage V_{peak} (the voltage for the peak current) was 1.3 V and the peak current density J_{peak} was 152 kA/cm^2. The peak-to-valley current ratio (PVCR) was 1.5×10^5. To our knowledge, this is the first observation to achieve J_{peak} over 100 kA/cm^2 and PVCR over 10^5 simultaneously for RTD, which is important for future application of high speed response and low power consumption.
Note also that the NDR characteristics can be reasonably explained by simple theoretical analysis of the I-V curve of an TBRTD using a ballistic transport model and by the transfer matrix method for the tunneling probability based on the effective mass approximation and the Esaki-Tsu formula for the calculation of the I-V curves[12] under the assumption that ΔE_C(CaF_2/Si) is around 1.5 eV, which is

35 % smaller than the bulk value. Figure 3(a) shows linear and (b) logarithmic plots of I-V curve from experiment and theoretical analysis considering serial parasitic resistance of 63 Ω. Experimental V_{peak} , J_{peak}, PVCR (~1.5×10^5) is well reproduced by calculation except leakage current at low bias voltage region, which is not considered in this study.
Actually, ΔE_C between bulk CaF_2 and Si is reported as around 2.3 eV, however, it seems that ΔE_C for atomically thin CaF_2 and Si reduced to be 1.5 eV[13]. One possible explanation of this shift is originated from the deviation of energy band structure formed under the assumption of infinite periodic lattice structure while only two periods of CaF_2 atomic layer (~0.62 nm) was used in this study.
The results obtained in this study clearly shows CaF_2/Si TBRTD structure has advantage for electron injectors or switches with both high-PVCR and -J_{peak} at least in principle, although further improvement is required to enable practical applications for nanoscale Si-LSI.

4. Conclusions

In conclusion, we have demonstrated room temperature NDR with high PVCR of 1.5×10^5 and with high peak current density of 152 kA/cm^2 using CaF_2/Si TBRTD structures grown on Si substrate. Two monolayer of CaF_2 (~0.62 nm) atomically thin layer was used for energy barrier and a few nm thick Si is used as quantum-wells. From the simulation, it was found that design and control of atomically thin barrier layers are the key for simultaneous achievement of high-PVCR and $-J_{peak}$, which are essential for applications of high speed response and low power consumption. NDR characteristics are reasonably reproduced by theoretical analysis using transfer matrix method based on ballistic transfer model. From the results of the simulation, it was strongly suggested that material parameters such as conduction band discontinuity (ΔE_C) should be modified from bulk value probably due to the deviation of energy band structure of a few monolayers.

The device concept based on the band engineering of artificial nano-heterostructures proposed in this study are a possible candidate for new scheme of electronic function for future LSI technologies aimed at ultimate scaling down to the atomic scale.

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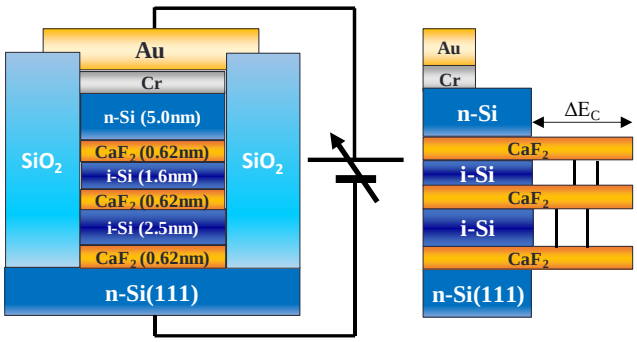

Fig. 1 Schematic cross section of the device structure and band diagram in flat band condition.

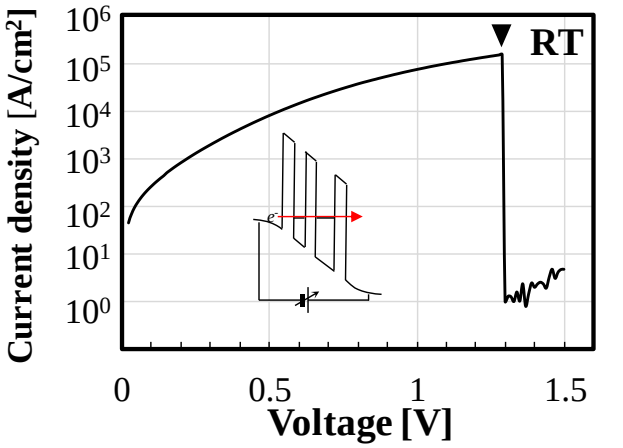

Fig. 2 Room temperature NDR characteristic of a CaF_2/Si TBRTD structure.

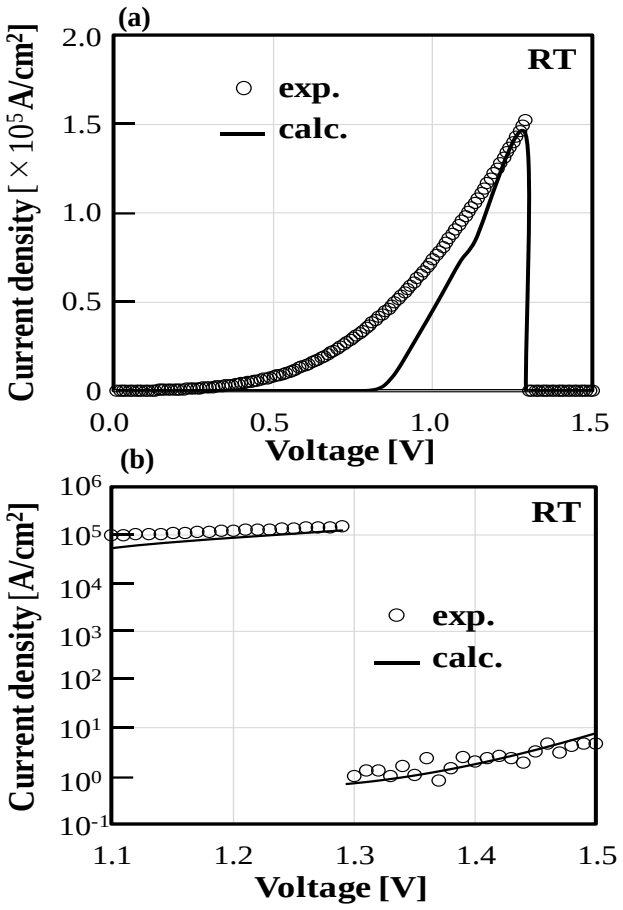

Fig. 3 Comparison between experimental and simulated I-V curves of CaF_2/Si TBRTD structure: (a) logarithmic and (b) linear plot.