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Reliable and Low Forming Voltage RRAM Enabled by Contact Shrinking and Pre-Soldering Baking

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Abstract

The requirements of RRAM (Resistive Random Access Memory) forming voltage reduction and post-soldering data integrity are met by novel processes including contact size reduction, WOx/TiOx thin film engineering, and the pre-soldering baking procedure. The WOx/TiOx RRAM device module is inserted between a contact W-plug and a Metal-1, with only one extra mask for defining the cell region. An 180nm 1Mb test chip is designed for statistical analysis down to 1ppm resolution. With the reduced contact and oxide film engineering, the forming voltage is successfully reduced from 3V to 2.2V with a high chip yield (>80%) even on a process developing wafer. The Ea of R change is 1.31eV and the data retention time can be >15 years at 80C. The pre-soldering baking procedure further increases the R window for high quality RRAM. An ultra-scaling technique further reduces the contact down to 28nm for improving array density without advanced lithography tools.

Introduction

Resistive random access memory (RRAM) has drawn much interest and has been a strong candidate for embedded memory applications because of its merits such as good retention, high speed, and good scalability, and, most importantly, low process cost [1-3]. Yet two issues still remain challenging for embedded applications: the high forming voltage [4], which may affect the RRAM macro size not only on the array dimension but also the supporting circuit design, and the data integrity after the soldering reflow especially in pre-programmed scenarios for most applications. This paper demonstrates effective ways to solve the above problems by novel integration schemes and a pre-soldering baking procedure. The proposed low-cost contact-reduction process and WOx/TiOx film stack successfully reduces the forming voltage from 3V to 2.2V. The >80% chip yield from the developing 1Mb test product further demonstrates the potential of the technology. A low cost, high precision 28nm contact ultra-scaling technique is also developed to improve the array density.

1Mb Test Chip Fabrication

A 1Mb WOx/TiOx RRAM chip (Fig.1) is developed based on a 180nm standard CMOS logic platform with an RRAM process module inserted between W-plug contact CMP and Metal-1(M1) deposition, with the flow shown in Fig.2. The RRAM process module starts with tungsten quality engineering. All the contacts are first recessed, filled with oxide spacer, and then followed by W-CVD / W-CMP to form the bottom electrode of the memory cell. The low aspect-ratio of the reduced contact ensures high quality W surface without any seam (Fig.6a). A plasma oxidation step to the reduced W plugs is then conducted, followed by depositing a thin Ti film as the ion scavenging layer. The resulting WOx/TiOx film stack establishes the core switching region of the memory cell. TiN top electrode is then deposited and patterned, with only-one additional photo step, to complete the RRAM module (Fig.6b-c). The peripheral contacts of the RRAM are etched away during top electrode patterning step such that the original contact plugs can be exposed, which ensures intact connection to CMOS. The TEM image in Fig. 4 shows drain/source contacts. The key parameters of the test chip are listed in Table I.

Electrical Characteristics

Fig.3 shows the reduction of forming voltage with contact size scaling primarily due to high electric efficiency from improved oxide quality. At the same time, thanks to the filamentary operation mechanism, the small variations on the size of the spacer-reduced contact rarely affect the switching performance. Fig.7 shows the resistance distribution of 1Mb WOx/TiOx RRAM chip. The high R state (HRS) and low R state (LRS) read window is up to 20 k-ohm with raw bit error rate (RBER) as low as 1E-6 after 100 RESET/SET cycles. An error correction circuit (ECC) in BCH (12, 8) scheme is good enough to guarantee for 500ppm product failure rate. Fig.8 shows the Sort-1 wafer map from a leading lot during process development. The 80% high chip yield indicates the potential of the low-cost RRAM process. The high temperature tests suggest the Ea for R change is 1.31eV and the data can be kept for >390 years and >15 years at 55C and 80C, respectively (Fig. 9). The WOx/TiOx RRAM provides a low cost embedded multiple-time program (MTP) solution.

Pre-Soldering Baking (PSB)

No failure was found from the full 1Mb chip test after the 260C soldering reflow process with the help of ECC; however, the read window is indeed overlapped at 1E-5 RBER. A proposed PSB (Fig.10) significantly improve the post-soldering R distribution at a 10 k-ohm HRS/LRS window even after 3 consecutive soldering processes, as shown in Fig.11. The PSB process can drive away weakly connected ions/vacancies by thermal energy, thus effectively screen out the weak cells at either HRS or LRS (Fig.12). These cells are then reprogrammed to ensure the filament quality.

Ultra-scaling Process

Since the switching layer of the proposed WOx/TiOx RRAM cell is in the reduced contact structure, the top electrode should fully cover the oxide layer to assure the device performance. The design rule concern of the memory cell is then actually the top electrode size variation and registration/rotation error from patterning process. A further reduced cell contact can not only improve oxide quality but also reduce the required size of top electrodes. An ultra-scaling technique is proposed in Fig.13. A TiN barrier is formed to serve as a sidewall protector during the SiO2 spacer-etching process. The sidewall TiN not only prevents lateral etching but also works as a collimator for the etching plasma. As a result vertical and small contact holes can be carried out down to 28nm without the expensive immersion 193 KrF photo-lithography process, as shown in Fig.14.

Conclusion

A novel WOx/TiOx RRAM technology is demonstrated on a 1Mb test chip. The requirements of forming voltage reduction and post-soldering data integrity are met by contact scaling, WOx/TiOx stack engineering, and the pre-soldering baking procedure. An ultra-scaling contact process utilizing the multi-functional TiN sidewall is further developed for 28nm RRAM device without advanced lithography tools, targeting at low-cost, high density array. With only one mask added, the WOx/TiOx RRAM technology provides a high-quality, low-cost embedded MTP memory solution suitable for almost all the fabs with W-plug process capability.

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References

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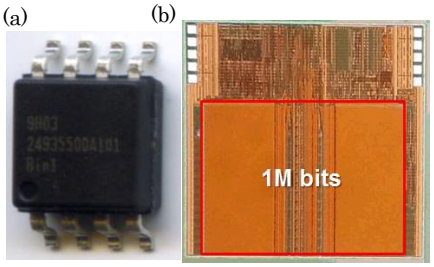

Fig. 1. (a) The 1Mb RRAM chip with standard SPI interface, and (b) die image.

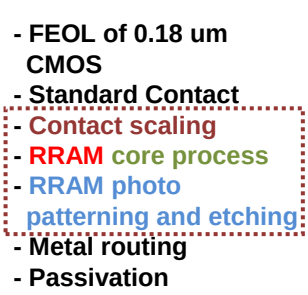

Fig. 2. RRAM process flow. The contact scaling technique and low cost RRAM core process are inserted between contact and M1.

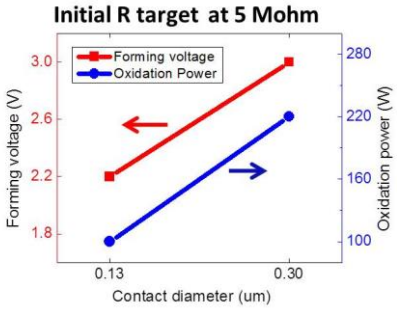

Fig. 3. RRAM process optimization among cell contact dimension, oxidation power, and the resulted forming voltage, targeting at an initial resistance 5 Mohm for best RRAM operation performances.

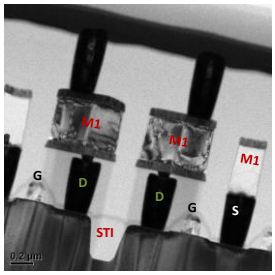

Fig. 4. TEM image of 1T1R structure. The drain-side memory cell in the array features scaled contact. The source side contact as well as all peripheral contacts remain normal.

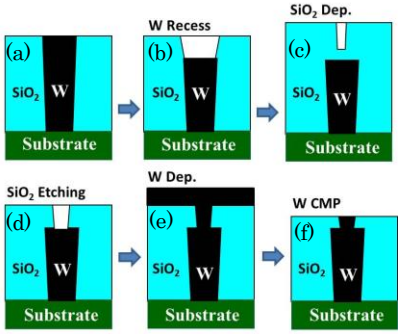

Fig. 5. Schematics of the major process steps for contact scaling and seamless W process. Thanks to the filamentary operation mechanism, the RRAM performance is improved even with the low-cost spacer contact scaling process that inherits size variation concerns.

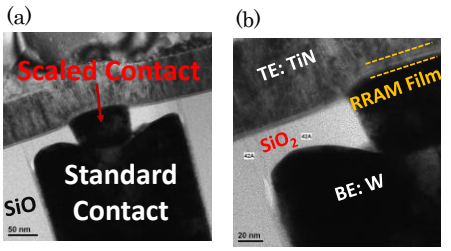

Fig. 6. TEM images of the RRAM core region. The RRAM cell is built on top of scaled contact structure with plasma oxidized TiO_x and WO_x formed between top (TiN) and bottom (W) electrodes.

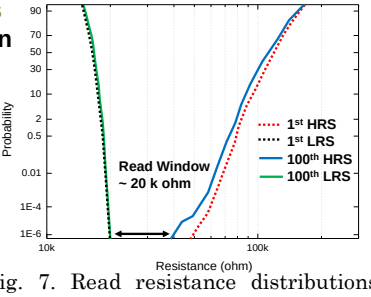

Fig. 7. Read resistance distributions from the 1Mb RRAM chip after electrical forming. The read window remains wide even after 100 RESET/SET cycles.

Process	0.18um
Reduced Contact	0.13um
Storage media	WOx /TiOx thin film
Capacity	1Mbits
Retention	80°C, 15 years
Raw Bit Error Rate	$< 10^{-5}$
ECC requirement for 500ppm product failure rate	BCH(12,8)
Endurance	> 100
Extra mask number	1

Table 1. Main features of the 1Mb RRAM based on 180 nm CMOS technology.

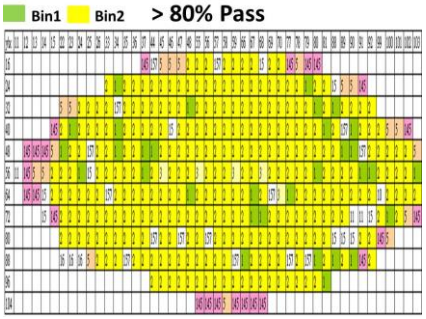

Fig. 8. The sort-1 map from the 8" wafer with scaled contact and oxide engineering. The chip yield is higher than 80%.

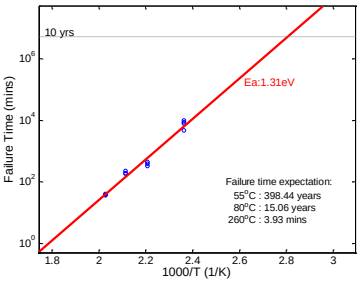

Fig. 9. Ea for R change is 1.31eV based on the statistics from the 1Mb TiOx/WO_x RRAM chip. Data retention is forecasted >390 yrs and >15yrs at 55°C and 80°C, respectively.

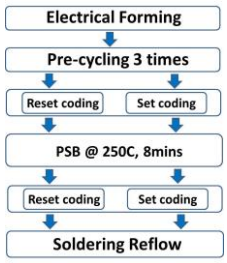

Fig. 10. The pre-soldering baking (PSB) procedure is designed to improve post-soldering R window. The PSB degrades the weak filaments for both RESET and SET states, and the follow up RESET and SET re-program those cells to ensure filament quality.

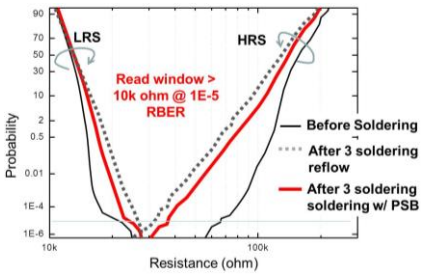

Fig. 11. The PSB effectively reduced the amount of R shift from the soldering process. Although ECC can fix the few error bits caused by 3 soldering processes (over-stressed condition), the proposed new flow can further widen up the window.

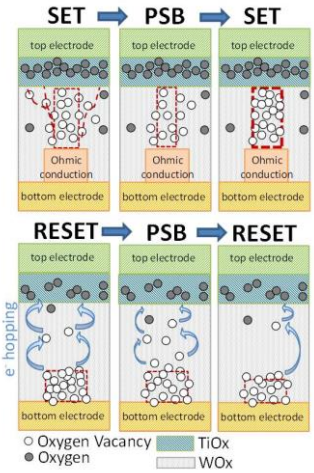

Fig. 12. Schematic operation mechanism of the PSB process. The PSB can drive-away vacancies in the weakly connected filament at SET state, or move-in vacancies close to the weakly disrupted filament at RESET state. In both cases the resistance level changes significantly and can be then re-programmed in the follow up verification test.

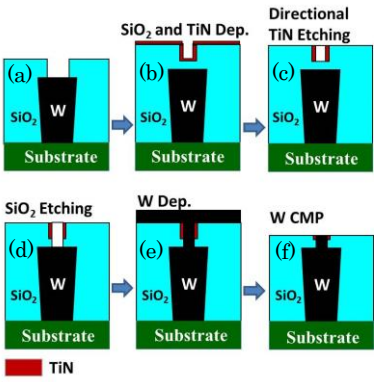

Fig. 13. Process flow of the aggressive ultra-scaling contact process. The thin TiN barrier serves as the side wall protector as well as plasma collimator during the spacer etching process.

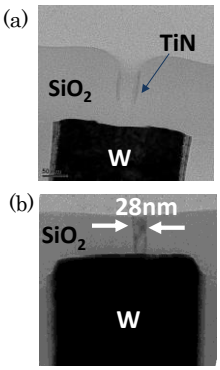

Fig. 14. TEM images of (a) the oxide spacer with TiN barrier at the side wall, and (b) the 28nm contact formed after the ultra-scaling spacer process.