Extended Abstracts of the 2018 International Conference on Solid State Devices and Materials, Tokyo, 2018, pp99-100

New Development and characterization of Oxide-based Selector for Cross-Point 25-nm ReRAM

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Abstract

In this paper, the authors report the outstanding performance from an innovative oxide selector for ReRAM (Resistance switching Random Access Memory). SiO_2 was chosen as a matrix oxide material and arsenic (As) metal atoms were implanted into the oxide films for threshold switching. Off-current and threshold voltage (V_{th}) could be controlled by process condition of As implantation. Finally its performance were verified by using 1S1R cross-point array.

1. Introduction

The limitation of scale-down of semiconductor technology in the near future requires next generation memories such as STT-MRAM, PCRAM, and ReRAM. One of these candidates, ReRAM has showed the satisfactory properties for wide range of application targets in terms of various characteristics.

High-efficient cross-point array can be realized by using a stacking of selector and resistor in order to control sneak current through unselected cells. Recently it has been reported that electrical metallization cells [1,2] and OTS (Ovonic Threshold Switching) selector [3,4] could be a good choice for non-volatile memory with the structure of cross-point array. However, there are several problems in applying the reported selectors to one selector-one resistor (1S1R) devices such as low threshold voltage, difficulty for reactive ion etch process, poor thermal instability, and so on. Therefore the development of new selector is essential to overcome these disadvantages and to achieve ReRAM chips with high-density cross-point array structure.

2. Experimental

SiO_2 film with the thickness of 10 nm was deposited on a TiN bottom electrode at first and then As atoms were injected into the SiO_2 film by using ion implantation method with adequate implant energy and dose. Consecutive fabrication processes followed by using 25-nm standard CMOS technology on 300 mm wafers. Figure 1 (a) shows the cross-sectional TEM image of an As-implanted SiO_2 selector cell. Typically selector performance has been measured by pulsed I-V with the pulse duration shorter than 1us. Finally array performance from 1S1R cross-point array was demonstrated with 16 Kb (128×128).

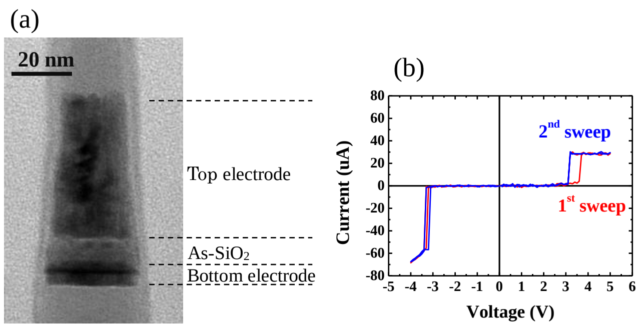


Fig. 1 (a) Cross-sectional TEM image and (b) I-V characteristics of As-doped SiO_2 selector.

2. Results

Figure 1 (b) shows a typical I-V curve representing electrical characteristics of the As-doped SiO_2 selector. Threshold switching can be observed even though the selector underwent high thermal budget as high as 400°C during the fabrication process. The device provides symmetric bi-directional volatile switching behavior even with different compliance current at both sides. The selector shows quietly low off-current of 80 pA at the half voltage of V_{th} in sub-threshold regime and abrupt change in current over V_{th}.

As shown in Fig. 2 of chemical state analysis of As-doped SiO_2 selector films, As atoms uniformly dispersed in SiO_2 matrix after the As implantation process. It's remarkable that most of As atoms remains in unoxidized state and small portion of Si-O bonds were broken into SiO_{2-x} due to the impact of the implantation of heavier As atoms.

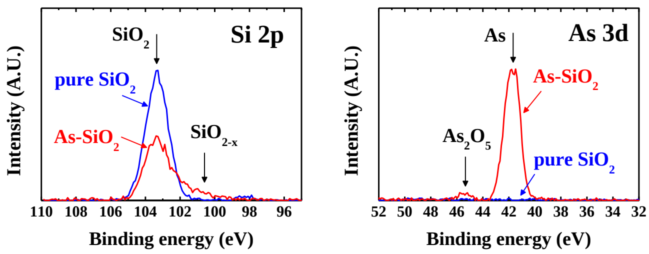


Fig. 2 XPS result of chemical bonding state of Si and As.

Electrical analysis was performed at various implantation doses of As to obtain better threshold switching performances. In the As concentration range of 90%~140% of reference concentration, all of devices showed good threshold switching characteristics in similar V_{th} and I_{off}. V_{th} and hold voltage (V_h) were characterized by using triangular pulse provided from a pulse generator. The median values of V_h and V_{th} are estimated to 3.0 V and 2.5 V, respectively.

It is exhibited that the device can quickly response to the applied voltage pulse in both of on-state and off-state. The transition time to on-state and off-state were measured to less than 52 ns and 23 ns, respectively, which are relatively faster than other selectors based on electrical metallization cell [1, 5]. This selector didn't show memory behavior even with 120 uA of input current. Consequently the new selector can supply high on-current density (J_{on}) upto 25 MA/cm^2 in sustaining selector characteristics.

It's well known that the increase of V_{th} with time can be easily observed in OTS selector consisted of disordered materials, which is harmful to device operation due to narrowing read window margin (V_{rd}). On the other hand As-SiO_2 selector didn't show any temporal change in V_{th}. The selector device can repeatedly switch more than 10^5 cycles in maintaining large on-off selectivity.

Figure 3 (a) shows the TEM image of the integrated 1S1R cell structure. The resultant short-pulse I-V of 1S1R device is shown in Fig. 3 (b). The half of V_{sw} is less than V_{th} of the selector so that it is expected that the 1S1R device can be switched to the both of set and reset state without sneak current through unselected cells.

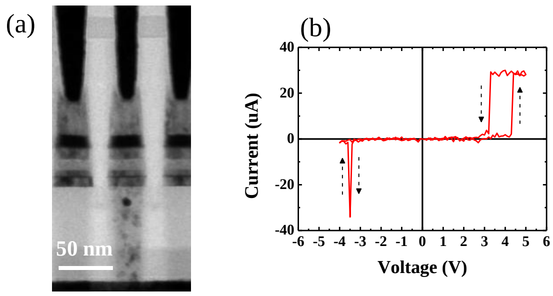


Fig. 3 (a) Cross-sectional TEM image and (b) I-V characteristics of 1S1R device.

The bit map image from 128×128 array shows that more than 92% of cells from the array can be switched to set and reset state in Fig. 4. The integrated 1S1R cell array shows wide sensing window between I_{LRS} and I_{HRS}.

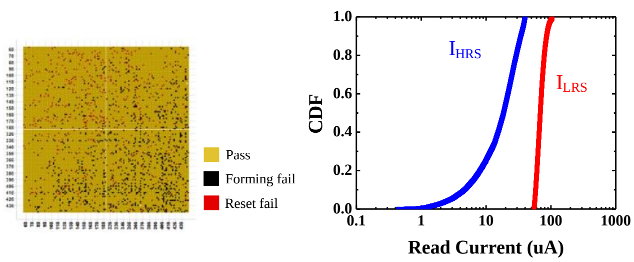
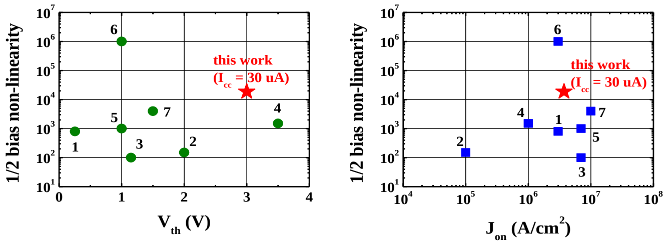


Fig. 4 Bit map image and cumulative distributions of the I_{LRS} and I_{HRS} of 128×128 array after set and reset programming at 25°C.

3. Conclusions

The experimental result showed that threshold switching and good off characteristics using non-mobile and fab-friend As-doped SiO_2 films can be obtained for cross-point ReRAM. The performance of integrated 1S1R cell was successfully demonstrated owing to the wide operating windows of current and voltage. Finally when compared with other selectors reported previously, As-SiO_2 selector revealed outstanding and reliable performances in terms of off-current, on-current, and V_{th} (Fig. 5).



1. IBM MIEC (VLSI 2011) [6]
2. Panasonic (ISSCC 2012) [7]
3. Samsung OTS (IEDM 2012) [8]
4. imec MSM (IEDM 2014) [9]
5. GIST Varistor (VLSI 2014) [10]
6. Crossbar FAST (IEDM 2014) [5]
7. imec OTS (VLSI 2017) [4]

Fig. 5 Comparison of J_{on}, V_{th}, and 1/2 bias non-linearity characteristics from various selectors.

References

[1] J. V. D. Hurk, *et al.*, *Volatile resistance states in electrochemical metallization cells enabling non-destructive readout of complementary resistive switches*, Nanotechnology, 25(42), 425202, (2014).

[2] R. Midya, *et al.*, *Anatomy of Ag/Hafnia-based selectors with 10^{10} nonlinearity*, *Advanced materials*, 1604457, (2017).

[3] S. R. Ovshinsky, *Reversible electrical switching phenomena in disordered structures*, Phys. Rev. Lett. 21 1450, (1968).

[4] B. Govoreanu, *et al.*, *Thermally stable integrated Se-based OTS selectors with >20 MA/cm^2 current drive >3.10^3 half-bias nonlinearity, tunable threshold voltage and excellent endurance*, VLSI Technology Digest, T92-T93, (2017).

[5] S. H. Jo, *et al.*, *3D stackable crossbar resistive memory based on field assisted superlinear threshold (FAST) selector*, IEDM Tech. Digest, pp.160-163, (2014).

[6] R. S. Shenoy, *et al.*, *Endurance and Scaling Trends of Novel Access-Devices for Multi-Layer Crosspoint-Memory based on Mixed-Ionic-Electronic-Conduction (MIEC) Materials*, VLSI Technology Digest, pp.94-95, (2011).

[7] Akifumi Kawahara1, *et al.*, *An 8 Mb Multi-Layered Cross-Point ReRAM Macro with 443 MB/s Write Throughput*, ISSCC Dig. Tech. Papers, pp. 432-434, (2012).

[8] M. J. Lee, *et al.*, *Highly-Scalable Threshold Switching Select Device based on Chaclogenide Glasses for 3D Nanoscaled Memory Arrays*, IEDM Tech. Digest, pp.33-35, (2012).

[9] L. Zhang, *et al.*, *High-Drive Current (>1 MA/cm^2) and Highly Nonlinear (>10^3) TiN/Amorphous-Silicon/TiN Scalable Bidirectional Selector with Excellent Reliability and Its Variability Impact on the 1S1R Array Performance*, IEDM Tech. Digest, pp.94-95, (2014).

[10] J. Woo, *et al.*, *Electrical and Reliability Characteristics of a Scaled (~30nm) Tunnel Barrier Selector (W/Ta_2O_5/TaO_x/TiO_2/TiN) with Excellent Performance (J_{MAX} > 10^7 A/cm^2)*, VLSI Technology Digest, pp.978-979, (2014).