

CMOS Compatible Germanium-based Bipolar RRAM

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Abstract

A germanium-based bipolar RRAM technology with excellent self-compliance and non-linear I-V characteristics is proposed and experimentally demonstrated. The RRAM is with a structure of TiN/HfO₂/GeO_x/n⁺-Ge substrate, which is highly compatible with standard CMOS processes and also shows the promising application in cross-point memory arrays.

1. Introduction

Resistive random access memory (RRAM) is one of the most promising emerging technologies for nonvolatile memory (NVM) [1, 2]. While most of RRAM devices with good resistive switching, endurance and retention behaviors show weak non-linear I-V characteristics under the low resistive state, resulting in sneak paths which could lead to additional reading power consumption and readout errors in the cross-bar array memory architectures [3, 4]. To overcome this problem, being integrated with a selector device such as diode (1D1R) [5] and transistor (1T1R) [6] has been proposed to suppress the crosstalk effect. However, the 1D1R and 1T1R structures increase the cell size and fabrication cost of RRAM. Furthermore, the integrated diode or transistor could also weaken RRAM's performance as the operating voltage is enhanced compared with the case of RRAM without a selector device [1]. In fact, selector devices will be not required for the memory array application if the RRAM device has both good bipolar resistive-switching behaviors and non-linear I-V characteristic [7]. Although several works about RRAM devices with the non-linear I-V characteristic have been reported [8-10], devices in the literatures show only the unipolar non-linear I-V characteristic, rather than the bipolar one, which does not meet the requirement for the application of selector-free RRAM array. Besides, a CMOS compatible RRAM technology is strongly needed upon considering the fabrication cost and the capability of integrating with the logic devices or circuits. Therefore, RRAM devices, which could be fabricated with a fully CMOS compatible technology, with the bipolar non-linear I-V characteristic is still in need for the memory array application.

In this work, we experimentally fabricated Germanium (Ge) based bipolar RRAM devices (TiN/HfO₂/GeO_x/n⁺-Ge), which could be processed with standard CMOS technologies. The devices exhibit good non-linear I-V characteristics, which are critical for suppressing the sneak paths and reducing the reading power in the selector-free cross-point array architectures.

2. Experiments

As shown in Fig. 1(a), a 100-nm-thick Al₂O₃ layer was used as the field oxide in order to decrease the leakage current and the area of resistive layer was $5 \times 5 \mu\text{m}^2$. The process fabrication is shown in Fig. 2. After a standard RCA wafer cleaning process, the field oxide was deposited using atomic layer deposition (ALD) at 300°C on the highly doped Ge wafer. Then, the field oxide was patterned by photo lithography and wet etching. Prior to the HfO_x and TiN deposition, a thin GeO_x layer was grown by ozone post oxidation. Then, the TiN electrode was patterned by the wet etching using Ni as a hard mask. Finally, Ni film was deposited as the back contact on Ge. The device cross section and materials were also confirmed by TEM (Fig. 1(b)).

3. Results and discussion

Fig. 3 shows the typical I-V characteristics of the bipolar set and reset processes of TiN/HfO₂/GeO_x/n⁺-Ge RRAM. The RRAM device shows a good self-compliance behavior in the set process. Furthermore, the 50X ratio of resistances read at V_{read} and $1/2V_{\text{read}}$ ($V_{\text{read}}=0.6$ V) performances a reliable non-linear factor (we call read ratio in this paper), which would effectively prevent leakage path in the cross-point array. A schematic of 3×3 cross-point memory array with V_{read} and $1/2V_{\text{read}}$ schemes is shown in Fig. 4. When the memory array reads selected cells using the V_{read} scheme, other cells are applied with $1/2V_{\text{read}}$ scheme. Obviously, the sneak paths would be effectively prevented due to the large ratio of resistances read at V_{read} and $\pm 1/2V_{\text{read}}$. It could help reduce the reading power consumption in the array architectures and suppress the readout errors. Large read ratios under different voltages as shown in Fig. 5 performance a promising potential application in the memory array integration. However, TiN/HfO₂/n⁺-Si device doesn't show any RRAM behaviors (Fig. 6) and we consider that the GeO_x interfacial should be critical for obtaining the resistive switching behaviors. The detailed mechanism of the resistive switching in Ge-based RRAM is still under investigation. As shown in Fig. 7-9, the TiN/HfO₂/GeO_x/n⁺-Ge RRAM device also shows excellent retention and endurance characteristics, which are very important for the future memory array application.

4. Conclusion

In this work, we proposed and experimentally demonstrated a CMOS compatible Ge-based RRAM, which shows not only good self-compliance behaviors, but also non-linear I-V characteristics. Thanks to the high rectifying ratio, the proposed Ge-based RRAM structure could effectively suppress the sneak path phenomena and reduce the reading power consumption in cross point memory arrays.

Acknowledgements

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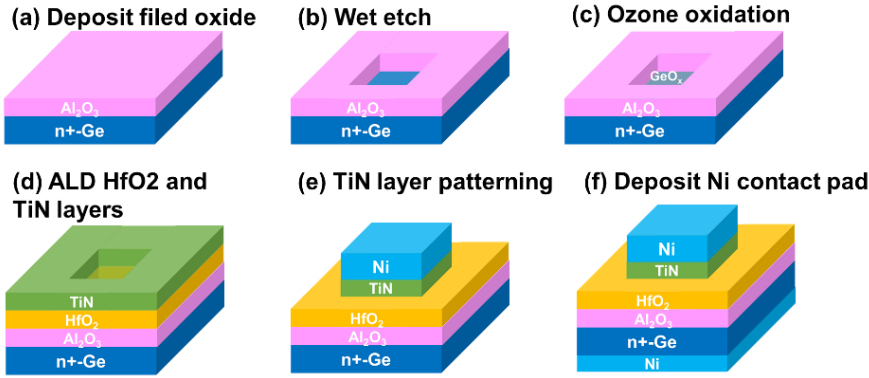


Fig. 2 Process flow of n^+ -Ge/ GeO_x / HfO_2 /TiN RRAM device.

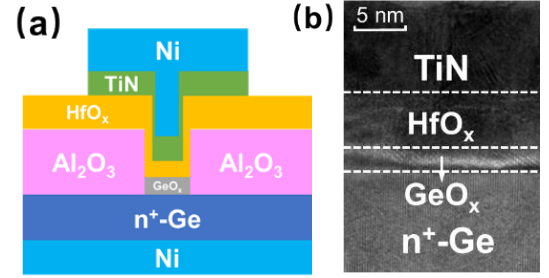


Fig. 1 (a) Schematic of the cross section and TEM image of n^+ -Ge/ GeO_x / HfO_2 /TiN RRAM.

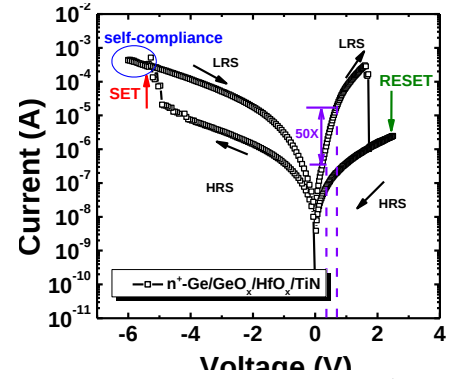


Fig. 3 I-V characteristics of n^+ -Ge/ GeO_x / HfO_2 /TiN RRAM in SET and RESET process.

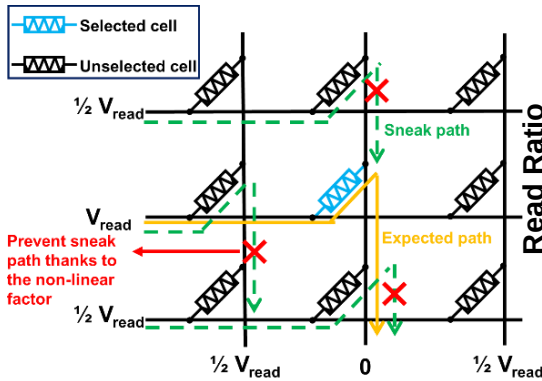


Fig. 4 Schematic of cross-point array with the V_{read} and $1/2 V_{\text{read}}$ scheme.

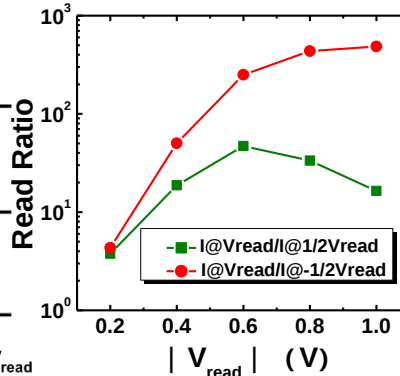


Fig. 5 The current ratios under V_{read} and $\pm 1/2 V_{\text{read}}$ as functions of $|V_{\text{read}}|$.

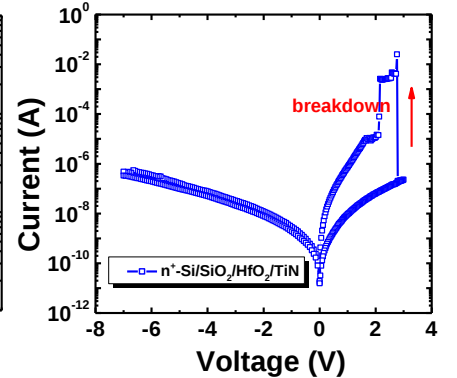


Fig. 6 I-V characteristics of n^+ -Si/ SiO_2 / HfO_2 /TiN RRAM.

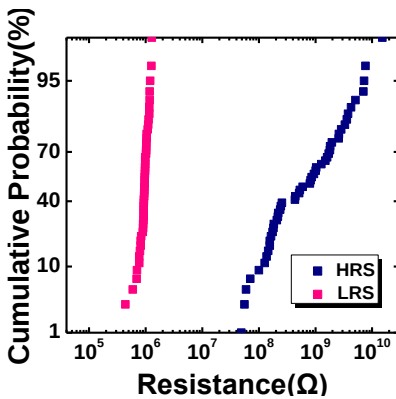


Fig. 7 The distribution of resistance at high resistance state and low resistance state.

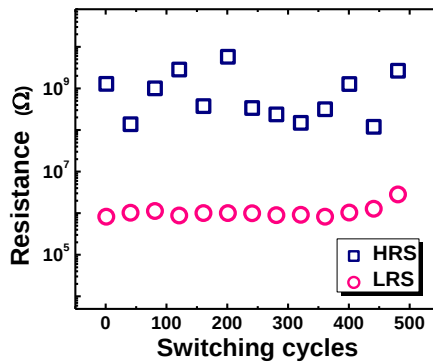


Fig. 8 Switching endurance of 500 cycles of n^+ -Ge/ GeO_x / HfO_2 /TiN RRAM.

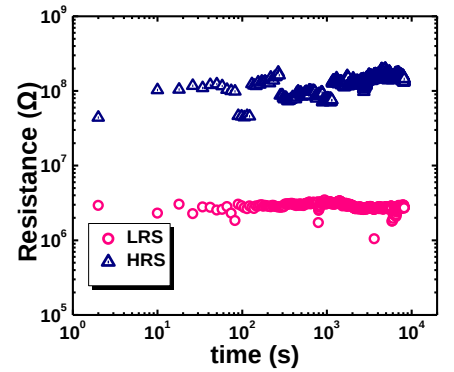


Fig. 9 Retention time over 10^4 s of the high resistance state and low resistance state.