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Capacitor-less Leaky Integrate and Fire Neuron Circuit Using Positive Feedback Field Effect Transistor for Low Energy Consumption

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Abstract

In this paper, we have fabricated the dual gate positive feedback field-effect transistor (FBFET) with the co-integrated CMOS and investigated DC and transient characteristics. The Fabricated FBFET has extremely low sub-threshold slope of less than 2.3 mV/dec and low off current. And we propose the CMOS analog integrate and fire neuron circuit using the FBFET that can significantly reduce the energy consumption by suppressing sub-threshold current. In addition, the floating body of the FBFET replaces the membrane capacitor that occupies a large area and performs leaky integration of the neuron, improving the circuit density and energy consumption by removing the capacitor.

1. Introduction

Recently, various type of the CMOS analog neuron circuits such as leaky I&F neuron, H-H neuron, log domain neuron and tau-cell neuron have been presented for implementing neural networks. In analog neuron circuit, most of the energy wasted by the sub-threshold current and the first inverter stage connected to the membrane capacitor consumes the largest percentage of the total circuit energy by the short circuit current. So the inverter has been called starved inverter [1]. Furthermore the capacitor occupies a large area and required additional devices for charging and dis-charging. To reducing energy consumption and circuit area, neuron circuit using non-volatile memory device such as RRAM, PRAM and IMT device are reported [2-4]. But these devices have endurance problems for use in neuron circuits.

In this work, we propose the analog neuron circuit using FBFET. The FBFET has attracted attention as a promising candidate for steep switching devices due to its superior subthreshold characteristics [5-6]. We designed the FBFET using two control gates and fabricated the device according to standard CMOS process. The FBFET completely suppresses sub-threshold current of the first inverter until switching occurs and replaces membrane capacitor function.

2. Results and Discussion

FBFET fabrication and measurement results

Fig. 1 shows the CMOS compatible fabrication process flow, device structure and SEM image of the FBFET. We designed the FBFET with $p^+n^-p^-n^+$-doped body and double gates. The gate1 controls the potential barrier of electrons and the gate2 makes potential well for charge integration. Fig. 2 shows the measurement result of I_d -V_{G1} characteristics according to the drain voltage. The FBFET has extremely steep switching characteristics with the subthreshold slope (*SS*) less than 2.3 mV/dec. And the drain current is constant after the FBFET is turned on, and increases exponentially as the V_{DS} increases linearly. Fig. 3 shows the transfer curves at various gate2 voltages. The threshold voltage increases linearly as the V_{G2} increases. The gate2 controls the depth of the potential well of the n-type body. The measurement result when voltage pulse is applied to gate1 is shown in Fig. 4. Every time the input pulse is applied to gate1, the electrons are accumulated in the floating body below the gate2, and as the amount of electrons increases sufficiently, the FBFET is turned on by the positive feedback between the electrons and potential barrier. The smaller amplitude of the pulse, the fewer electrons are accumulated in the floating body, so the larger number of pulses is required to turn on the FBFET.

I&F neuron circuit with FBFET

Fig. 5 illustrates the proposed neuron circuit diagram. The first inverter consists of the FBFET and a p-type MOSFET, and the FBFET performed temporal integration function. To verify the circuit operation, circuit simulation was performed by the mixed mode smart spice. The simulation results are shown in Fig. 6 ((a) charge concentration in the floating body of the FBFET, (b) each node bias, (c) drain current of the FBFET, (d) drain current of the first inverter in conventional neuron circuit). The input pulses are integrated by the electrons accumulating in the floating body of the FBFET. And leaky integration is performed by electron recombination. When the number of electron is exceed the threshold point, the hole concentration in the floating body below the gate1 increased abruptly, and the FBFET turned on very fast. During the accumulation of electrons, sub-threshold current is completely suppressed. The drain current flow only in short moments when the first inverter switching occurs. Then the node1 is discharged to ground and the FBFET turned off. Finally the output pulse is generated and accumulated charges are removed by recombination. In conventional neuron circuit, during the membrane capacitor is charged, the sub-threshold current continues to flow and the most of energy consumed at this period. The energy consumed in the first inverter during 14μs is 5.4pJ for the FBFET neuron circuit and 56.1pJ for the conventional circuit. The energy consumption of the first inverter is reduced by 90 % by using

FBFET. Furthermore, the total area of the neuron circuit is greatly reduced by removing membrane capacitor and additional devices for charging and discharging the capacitor.

3. Conclusions

In this work, we have fabricated the dual gate FBFET and investigated DC and transient characteristics. The Fabricated FBFET has extremely low sub-threshold slope of less than 2.3 mV/dec and low off current. And we propose the analog integrate and fire neuron circuit using the FBFET. In the proposed neuron circuit, the sub-threshold current is significantly suppressed by adopting the FBFET in the first inverter. And by replacing the function of the membrane capacitor with the FBFET, the cell area is greatly reduced.

Acknowledgements

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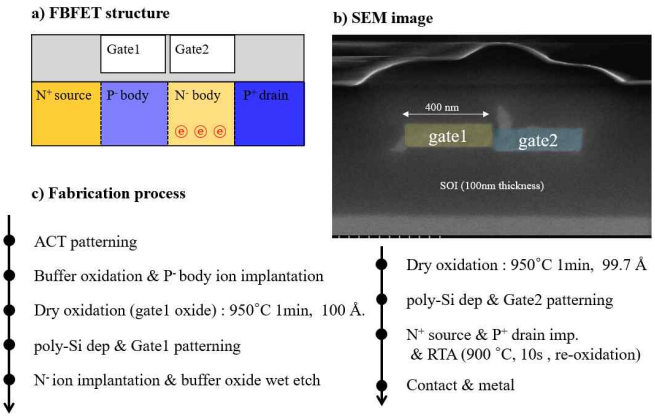

Fig. 1. (a) Device structure, (b) SEM image, and (c) CMOS compatible fabrication process flow the FBFET.

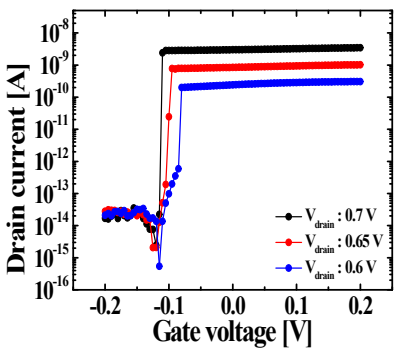

Fig. 2. Measurement of Id-Vg1 curves according to drain voltages. The sub-threshold swing is 2.3 mV/dec at drain bias is 0.7 V.

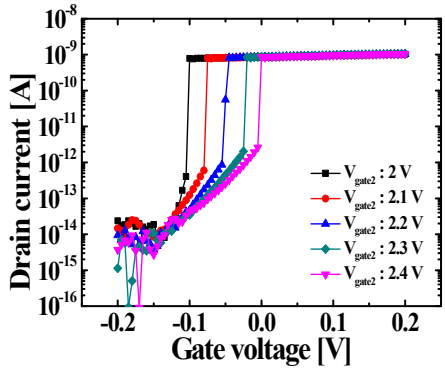

Fig. 3. Measurement result of Transfer curves at various gate2 voltages. Threshold voltage is linearly increased by the gate2 bias.

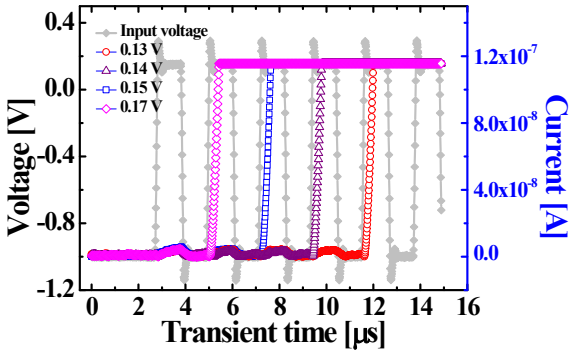

Fig. 4. The measurement result when pulse train is applied to various amplitude of the gate1 voltage.

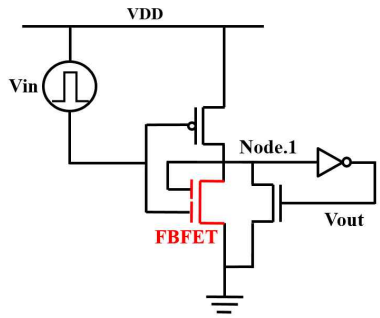

Fig. 5. Proposed neuron circuit with FBFET diagram.

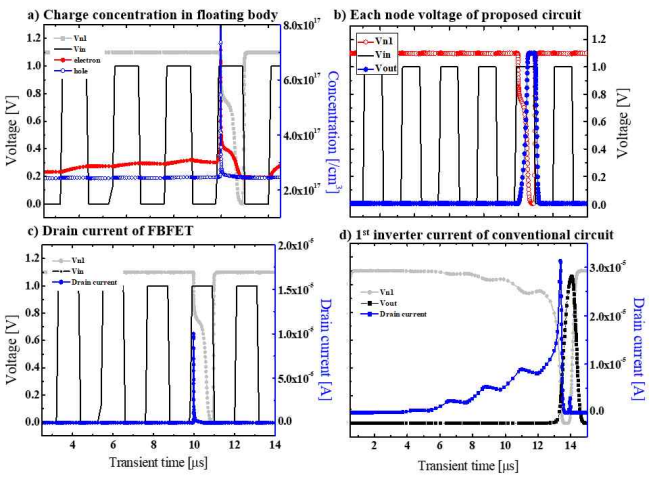

Fig. 6. The spice simulation results (a) charge concentration in the floating body of the FBFET, (b) each node bias, (c) drain current of the FBFET, and (d) current of the 1st inverter in conventional neuron.