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Characterization and Modelling of Analogue FTJ Memristors as Artificial Synapses for Neuromorphic Systems

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Abstract

Analogue memristors represent promising candidates for implementation as artificial synapses in neuromorphic systems. Compared with filamentary-type memristors, ferroelectric-tunneling-junction (FTJ) capacitors have been seldom studied in the context of analogue behavior. In this paper we present a pulse measurement study on the analogue switching behavior of HfSiO FTJ memristors. We show initial device state uniformity, good scalability, ultra-low current operation and accurate analogue conductance switch modelling, all necessary device characteristics required for implementation as artificial synapses. We conclude our study with an experimental demonstration of a simple FTJ-based neural network implementing Hebbian learning.

1. Introduction

In the context of neuromorphic engineering, emerging non-volatile memristive synapses can be used as the learning element, storing learned features of incoming data while also performing computation at the location of the memory, drastically decreasing power consumption promoted by the intrinsic non-von-Neumann architecture of the system [1]. For successful adoption, artificial synapses employed in such circuits have a minimum set of requirements: nano-scale size, low-current operation, low device operation variability and analogue predictable switching under pulsing input [2].

Recently, analogue FTJ devices have received some attention as their gradual switching behavior is akin to memristive dynamics [3] and can offer promise in implementation as artificial synapses in neuromorphic systems. Usually, FTJ devices exhibit binary switching, where the ferroelectric layer (FE) is maximally polarized in one direction to achieve binary operation (Fig. 1a) [4]. However, under controlled pulsing, partial domains of the FE layer can be gradually switched and such allowing continuous modulation of the tunneling current across the device (Fig. 1b). Past efforts have shown partial characterization of CMOS-incompatible devices [3].

We present a pulsing study on HfSiO FTJ nano-scale memristive synapses (Fig. 1c) showing promising behavior suitable for inclusion as artificial synapses in neuromorphic systems.

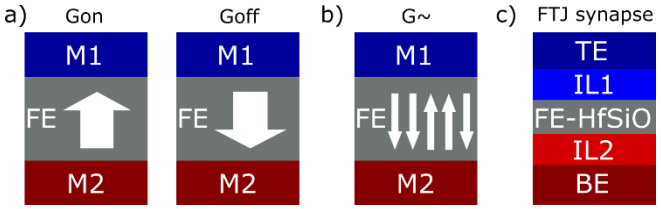

Fig. 1: a) Maximally polarized FTJ device illustration for binary operation; b) Partially polarized FTJ device for analogue operation; c) Proposed FTJ memristive synapse structure.

2. FTJ Pulse-based Characterisation

Our device structure is represented in Fig. 1c. For this study we characterized 24 devices with feature sizes of 150, 160, 180, 200, 300 and 500 nm. Throughout our study, the device under test was measured at 2V after each applied pulse.

Our pulsing strategy involved an initial spot reading and I-V sweeping, followed by repeated pulsing with a maximum positive amplitude for our study (5V), followed by negative pulsing with same amplitude. The purpose is to find soft boundary G_{on} and G_{off} states which we then use in a subsequent pulsing algorithm which scans the conductance-pulse-amplitude (G-V) space to record the effect of several pulse amplitudes based on initial conductance state.

Fig. 2a shows initial state distributions for all device sizes and non-switching I-Vs. Fig. 2b,c shows two stages of biphasic repeated pulsing with same amplitude. The initial state distributions are narrow and pulsing response is reproducible over devices of same size.

Fig. 2d shows an example measurement result of our G-V pulsing algorithm for a 200 nm FTJ synapse. Each marker represents relative conductance switch for one pulse with amplitude Vp (1µs) and initial conductance G_0. The device exhibits soft SET and hard RESET. Nonetheless, gradual conductance modulation is possible in both directions by using asymmetric voltage pulse amplitudes (higher for SET than RESET). We model the G-V space by eqs. (1)-(2) relating to positive (potentiating), and negative (depressing) relative conductance switch transitions, respectively.

$$\Delta G_+(V, G_0) = e^{K_{VP}(V-V_P)} * \left(1 - \frac{1}{1 + e^{-K_{GP}(G_0 - G_P)}}\right) \quad (1)$$

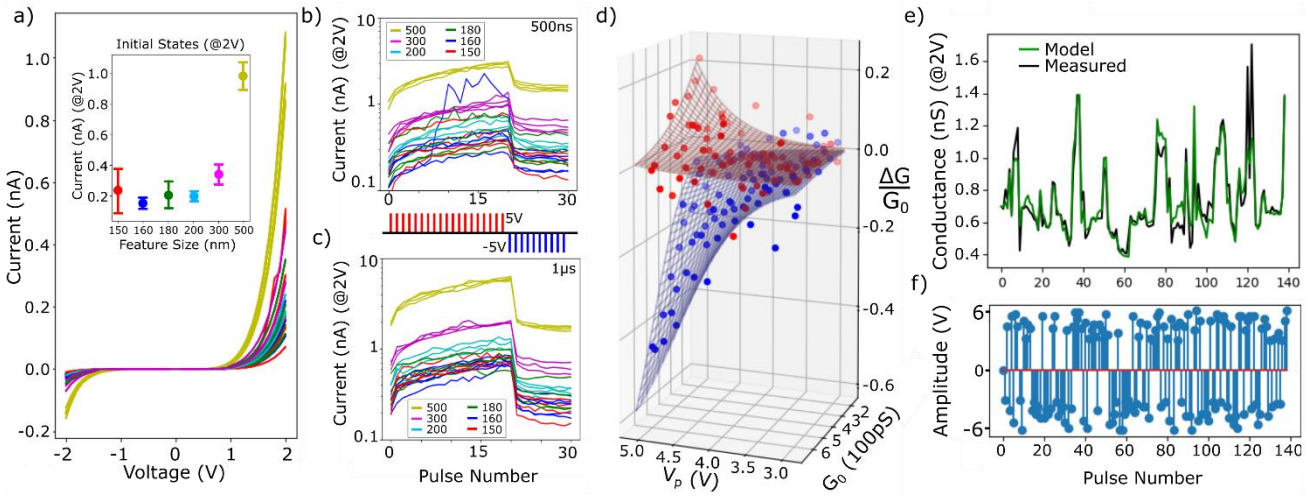

Fig. 2: a) Initial IV sweeps of 24 measured FTJ synapses; inset – distribution of initial conductance states measured at 2V; b) Convergence pulsing with 5V, 500ns followed by -5V 500ns for all devices; c) Convergence pulsing with 5V, 1 µs followed by -5V 1µs for all devices; Insets show device size in nm; d) G-V pulsing measurement results for a 200nm FTJ synapse fitted with model from eqs. (1)-(2); RED marks potentiating pulses (positive V_P), BLUE marks depressing pulses (negative V_P); e) Random pulsing run for device in d) with model evolution starting from same conductance state showing good agreement with measured data; f) Pulses applied to device in e) (1 µs).

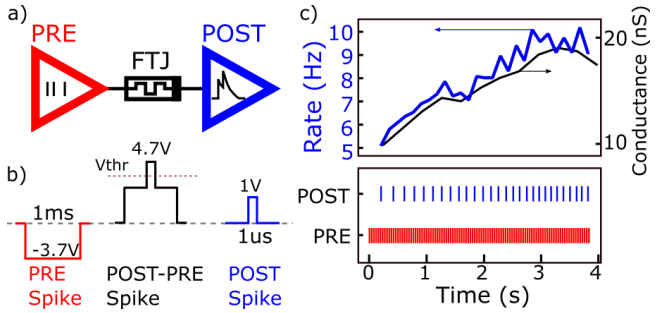

Fig. 3: a) Hebbian learning experiment circuit illustration: PRE-synaptic neuron spiking at a fixed rate of 500 Hz; POST-synaptic leaky integrate and fire neuron with membrane τ=1s and threshold voltage of 60mV; FTJ synapse of size=500nm; b) PRE and POST synaptic spike shapes; c) top: POST-synaptic instantaneous rate increasing over time and FTJ synapse conductance increasing over time as a consequence of PRE firing POST; conductance measured at 3.7V; bottom: raster plot of PRE and POST-synaptic spike times.

$$\Delta G_{-}(V, G_0) = \frac{-1}{1 + e^{-K_{VD}(V - V_D)}} * \frac{1}{1 + e^{-K_{GD}(G_0 - G_D)}} \quad (2)$$

where ΔG represents relative conductance switch from G_0 after a pulse with amplitude V, and K_{VP}, V_P, K_{GP}, G_P, K_{VD}, V_D, K_{GD} and G_D are dimensionless optimization parameters.

We test our fitted model against a pulsing run with random amplitudes on the same device. The model is initialized with the start conductance state of the FTJ device and is updated based on received voltage pulse. The respective pulsing run is shown in Fig. 2e showing excellent model agreement. We note that the random pulsing run employed amplitudes up to 6V, whilst our model was fitted on data taken for pulsing up to 5V, validating the robustness of our model.

3. FTJ based Hebbian-learning

Weight update in neuromorphic systems, and similarly synapse update and hence learning in the brain, is only performed via the local activity of neighbouring neurons. We demonstrate a simple spiking neural network operating in real time consisting of a pre-synaptic spiking neuron and a leaky integrate and fire post-synaptic neuron (Fig. 3a). The network illustrates the concept of Hebbian associative learning [5], where correlated neuron spiking activity potentiates connecting synapses. We employ a FTJ analogue memristor as the synapse and show that through repeated spiking of the post-synaptic neuron induced by spiking of the pre-synaptic neuron, the post-synaptic rate increases over time as a consequence of the potentiation of the FTJ synapse (Fig. 3c). This is achieved by tailoring the pre- and post-synaptic pulse shapes (Fig. 3b) based on our previous modelling.

4. Conclusions

We have presented a study on the characterization of FTJ memristive synapses with analogue conductance switching. Our devices show nS range conductance and low device variability making them suitable for implementation in emerging neuromorphic systems. We have proposed a model which accurately fits the FTJ pulsing response even under random pulsing (random spiking). A simple application was demonstrated experimentally validating the analogue operation of FTJ memristive synapses in artificial spiking neural networks.

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