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Prospects of Nonvolatile Logic LSI Using MTJ/MOS-Hybrid Circuitry and Its Application

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Abstract

Magnetic-Tunnel Junction (MTJ)-based non-volatile logic-circuit LSIs have some possibility to solve the power-dissipation problem seriously focusing on the present CMOS-only-based VLSI processors. In this paper, some recent results concerning logic-circuit LSIs using MTJ/MOS-hybrid circuitry are reviewed, and their impact such as reliability enhancement like "die-hard" LSI is discussed through the concrete examples.

1. Summary

In the present CMOS-only-based VLSI, there are several serious problems such as communication bottleneck between memory and logic modules inside a VLSI chip, increasing power dissipation, especially standby power dissipation, and device-characteristic variation effect. Recently in the Internet of Everything (IoE) era, it is accelerated to reduce the power dissipation in LSI chips, while still increasing high-performance processing capability.

On the other hand, several emerging storage devices are getting developed to overcome the weak points of ordinary semiconductor memories; dynamic random-access memory (DRAM) and static random-access memory (SRAM). Especially, magneto-resistive random-access memory (MRAM) that has already undergone a few incarnations, is now converging on a scheme for upending the memory business. Spin-transfer torque (STT) MRAM promises speed and reliability comparable to that of SRAM, where SRAM is the quick-access memory embedded inside microprocessors, along with the "non-volatility" of flash, the storage of smartphones and other portables [1-2]. Since magnetic tunnel junction (MTJ) device, the key element of MRAM, is easily distributed over a logic-circuit plane by using a three-dimensional (3D) stack structure, performance degradation due to intra-chip global wires could be drastically mitigated, which could be lead to a high-performance, ultra-low-power and highly reliable (or highly resilient) logic LSIs [3-5].

One of the most useful methods to cut off leakage power is to use power gating. If the power gating is applied in the conventional CMOS-only-based logic LSI, almost all the standby power can be surely eliminated, but two additional operations, "back-up" and "boost-up" procedures, must be additionally applied before and after utilizing the power gating, respectively, which may discourage to apply the power-gating technique. In contrast, the use of nonvolatile devices as storage elements maximizes the merit of power saving due to the power-gating technique. Since a judicious combination between nonvolatile devices and the power-gating technique has been naturally realized in the MTJ-based nonvolatile VLSI-processor architecture, it is truly expected that the wasted power dissipation could be ideally eliminated. In order to accelerate the implementation of nonvolatile logic LSIs, you must make efforts to develop key technologies in every LSI-design hierarchy from device/material level to system-architecture/application level [3].

As concrete examples of such nonvolatile logic LSIs, self-terminated nonvolatile flip-flops (NV-FFs), which make it possible to minimize the write energy for MTJ devices by monitoring the voltage change in MTJ switching and terminating write current, has been proposed [6-8]. Figure 1(a) shows the schematic diagram of the self-terminated NV-FF. Figure 1(b) shows the comparison of nonvolatile storage cells using the 2T-MTJ device and the 3T-MTJ device. In case of 3T-MTJ-based nonvolatile storage cell, the read-operation path is separated from the write-operation path, which makes it possible to relax design space exploration. By utilizing the self-terminated mechanism, the backup energy consumption is greatly reduced. In fact, the average backup energy is reduced by 69% compared with that of a conventional non-self-terminated method.

A new design flow for MTJ/MOS-hybrid LSI considering stochastic behavior of MTJ devices has been also established by combining new supplementary design libraries that reflect the physical behavior of MTJ device and de-facto standard EDA tools [9-11]. By utilizing the proposed flow, various MTJ-based nonvolatile logic-in-memory (NV-LIM) circuits can be designed with Verilog Hardware Description Language (Verilog-HDL). Their operation including the effect of MTJ's stochastic switching behavior can be verified by analog-mixed-signal (AMS) simulation. Figure 2 shows a layout of the microprocessor with 90nm MOS/100nm perpendicular MTJ technology generated by the proposed flow, whose layout validity can be completely verified through DRC and LVS using standard EDA tools. The processor is based on a general purpose 32-bit microprocessor (ARM Cortex-M0), where all flip-flops in it are replaced with nonvolatile flip-flops to add non-volatility.

Finally, it is also important to use MTJ/MOS-hybrid nonvolatile logic-circuit style not only in a standard synchronized computer system, but also in an asynchronous one, because of accelerating the usefulness of the power-gating technique [12]. In addition, the nonvolatile logic-circuit style is useful

not only in reducing the power dissipation, but also in enhancing the reliability. Some concrete approaches for achieving sudden power-outage resilience have been proposed [13-16].

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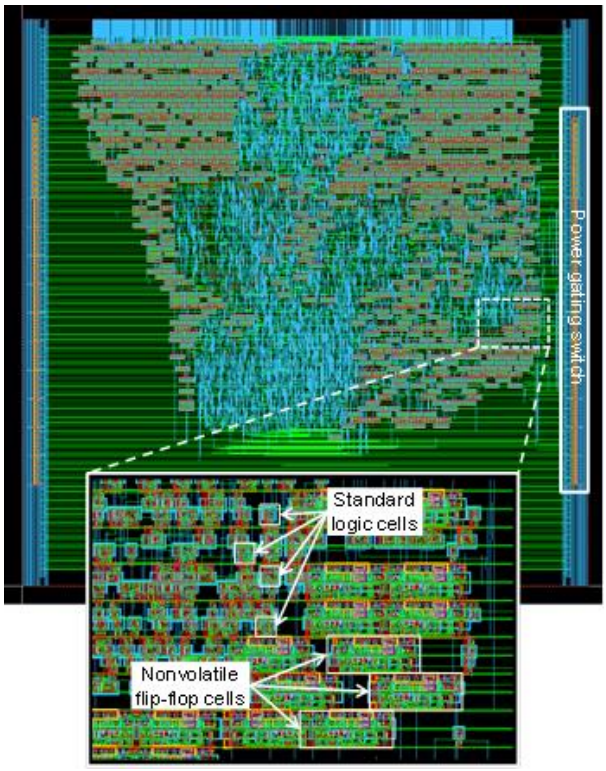

Fig. 2: Layout of experimental nonvolatile microprocessor, where an automated VLSI CAD tool is established for MTJ/MOS-hybrid logic-circuit design.

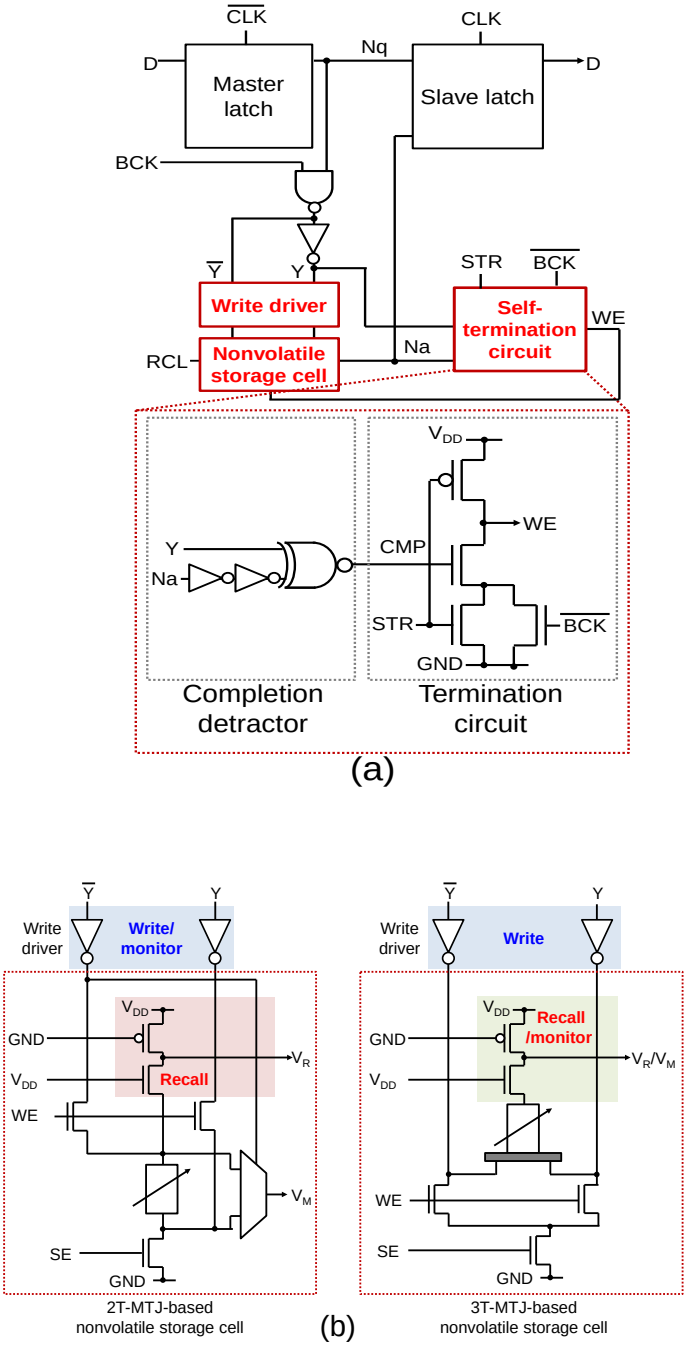

Fig. 1: Design of a self-terminated nonvolatile flip-flop; (a) overall schematic, and (b) nonvolatile storage cell configurations with two-terminal (2T) and three-terminal (3T) MTJs, respectively.