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Integration of Low-k Low Temperature 400°C SiCO as Offset Spacer in view of 3D Sequential Integration

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Abstract

In this paper, the interest of low-k, low temperature SiCO deposition at 400°C as offset spacers is highlighted through FDSOI MOSFETs low temperature process integration. The excellent material and electrical properties as compared to SiN 630°C POR reference, ensures the integrability of SiCO for 3D VLSI integration and its interest for advanced nodes.

1. Introduction

3D sequential CoolCube™ integration is based on stacked layers of devices fabricated one on top of each other, allowing very small 3D contact pitch (limited only by lithographic performance) and gains in power and performance [1] (Fig.1.a)). However, this integration faces the challenge to realize a high performance transistor at the top level without impacting the electrical characteristics of the bottom one. One of the issues consists in integrating transistors with low temperature process steps. Bottom MOSFET tolerable thermal budget, to prevent silicide instability has been evaluated for state of the art advanced planar FDSOI technology with ultra-thin film [2] and summarized in Figure.1b) [1]. The maximum top FET temperature is fixed at around 500°C 2h. One of the critical step in CMOS integration is the formation of offset spacers in order to isolate the gate stack from raised sources and drains. Actual process of reference (POR) for offset spacer material is silicon nitride (SiNx) deposited at 630°C by Atomic Layer Deposition (ALD). Therefore, it becomes necessary to investigate new materials which not only fit with the limited thermal budget constraint as demonstrated in our previous work [3-4], but also meet the low temperature integration requirements with a low-k value for fringe capacitance reduction in advanced nodes.

In this work, we investigate for the first time the SiCO deposited at 400°C by CVD to replace the 630°C SiN POR as offset spacers in a low temperature FDSOI CMOS process flow.

2. Experimentals

SiCO films were deposited at 400°C on 300mm wafers in Lam's Striker Carbide chamber. Films were first deposited on blanket wafers to characterize the dielectric properties. Measurements were performed on as-deposited films and after a 600°C 15min furnace anneal in order to simulate subsequent epitaxy step thermal budget (which was overestimated here compared to the targeted low thermal budget process flow) and evaluate the thermal stability of the dielectric. Then, SiCO was integrated in a standard planar FDSOI CMOS following the process flow given in Fig. 2. The final anneal is either 1050°C high-temperature (HT) spike as reference or 600°C 2min low temperature (LT) in case of Solid Phase Epitaxy Regrowth (SPER) [5] for dopant activation and source/drain recrystallization. The electrical results were compared to transistors fabricated with POR SiN 630°C offset spacers.

3. Material & electrical characterization

Refractive index (RI), density and stress for as-deposited and annealed films given in Table I show good stability of SiCO against a 600°C 15min annealing. This is also highlighted by the FTIR measurements after annealing, showing no modification of the spectrum (Fig.3). Using an Hg probe, low permittivity of k=4.5 was measured, showing the interest for the dynamic performances as well as compared to POR SiN (k~7). Additionally, very low leakage (2.10^{-9}A/cm² at 2MV/cm) and high breakdown voltage (7.7MV/cm) were obtained.

4. CMOSFET integration

SiCO was then integrated as offset spacer between gate and raised source and drain. TEM observations on LT annealed PMOS at process end reveal a spacer length of 9 and 10nm respectively for SiCO and POR SiN (Fig.4). The spacer etch of both SiN and SiCO by standard RIE (Reactive Ion Etching) recipe is followed by Si raised source/drain epitaxy with selectivity preserved over the dielectric (Fig. 5 for SiCO). Similar Ion/Ioff trade-off, short channel effects were thus obtained on HT NMOS (Fig. 6a), b), c)). The slightly higher SCE and DIBL for the SiCO is only due to its smaller CD value (<1nm) as compared to the SiN one. This effect is confirmed by the lower extracted access resistance for both NMOS ($R_{SD/POR}$=137Ω.cm; $R_{SD/SiCO}$=125Ω.cm) (Fig.7). EOT (0.8nm) Fig.8, and mobility versus gate length in linear regime are similar for both materials, indicating no impact of SiCO on the carriers mobility (Fig. 9). Regarding the PMOS, similar conclusions are highlighted for the HT anneal variants (Fig.10a), b), c)). The variants with low temperature SPER dopants activation reveals stronger short channel effects due to a non-fully optimized dopant implantation in the access region (Source and Drain). That will be optimized in future works. However, the Ion/Ioff trade-off are similar as compared to the both SiCO and SiN HT one attesting the viability of this spacer in view of low-k low-temperature process integration.

5. Conclusion

We demonstrated for the first time the integration of low temperature SiCO deposited at 400°C in both standard (HT) and low temperature (LT) anneal CMOS FDSOI process flow. Good stability versus thermal annealing ensured the physical and electrical integrity of the dielectric throughout the integration. Equivalent static performance (Ion/Ioff trade-off, SCE, DIBL, access resistance, EOT, mobility) were obtained, raising the interest of SiCO as low-k and low temperature offset spacer in view of 3D sequential integration.

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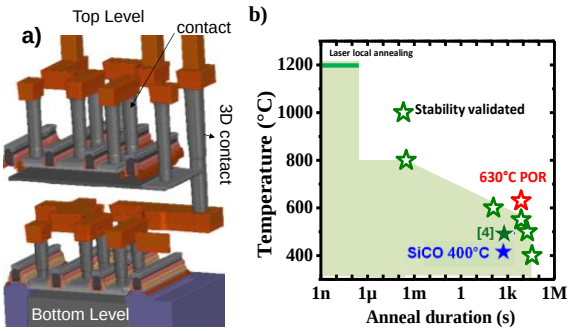


Fig.1: a) Coolcube^{TM} integration **b)** Bottom MOSFET stability versus thermal budgets [1].

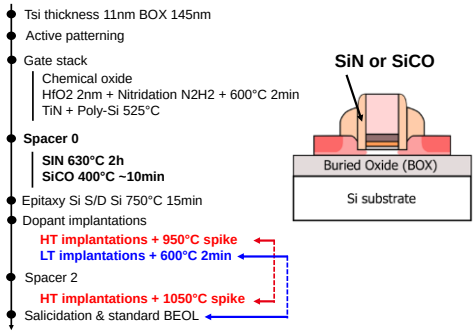


Fig.2: Process flow scheme of CMOS transistors on FDSOI.

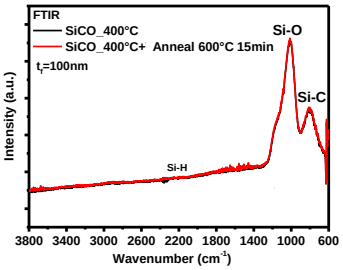


Fig. 3: FTIR spectra for as-deposited and annealed SiCO.

	SiCO	
	As-dep	**600°C 15min**
RI@633nm	1.66	1.66
Density (g.cm-3)	2.19	2.26
Stress (MPa)	+50	+175
Shrink	/	-0.5%
k	4.5	4.5
J@2MV/cm (A/cm²)	2.0^{E}-9	/
Vbd (MV/cm)	7.7	/

Table I: Properties and composition of as-deposited and annealed 600°C 15min SiCO.

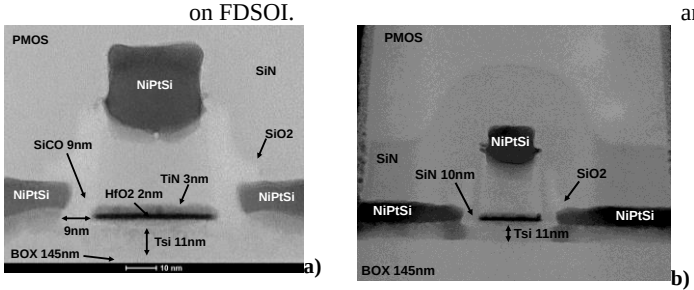


Fig.4: TEM observations of PMOS at process end for a) SiCO spacers and b) SiN spacers annealed at low temperature (LT).

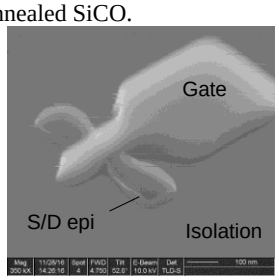


Fig. 5: SEM observation after raised SD epitaxy showing good selectivity over SiCO.

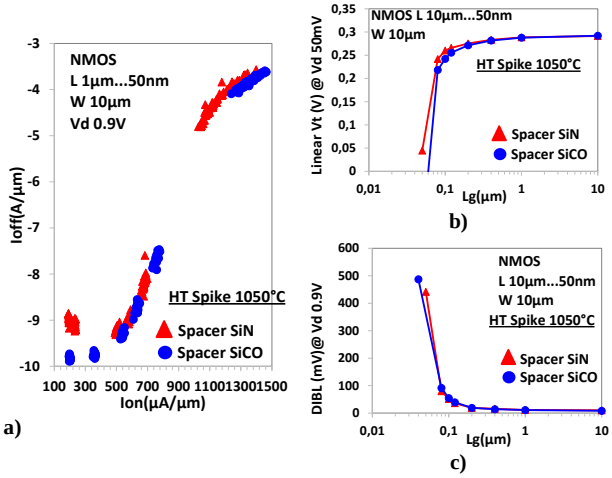


Fig.6: NMOS **a)** Ion/Ioff trade-off **b)** Linear Vt(L) **c)** DIBL(L) for HT anneal SiN and SiCO spacers.

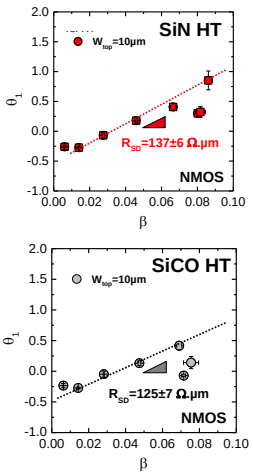


Fig.7: NMOS access resistance extraction for HT anneal SiN and SiCO spacers.

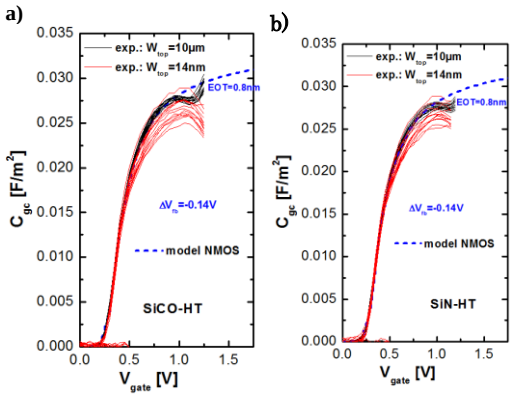


Fig.8: EOT extraction for HT SiCO (a) and HT anneal SiN variants for two channel widths.

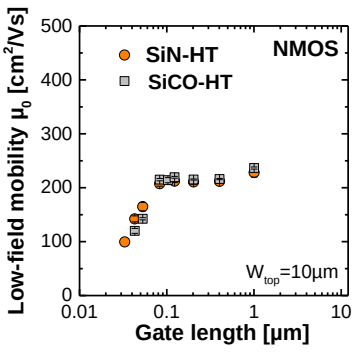
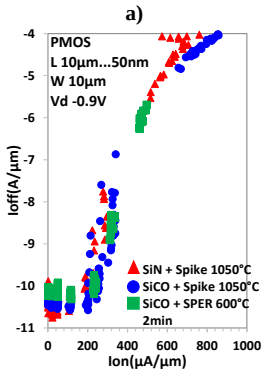


Fig.9: NMOS µ(L) in linear regime for the two offset spacers @ HT anneal.



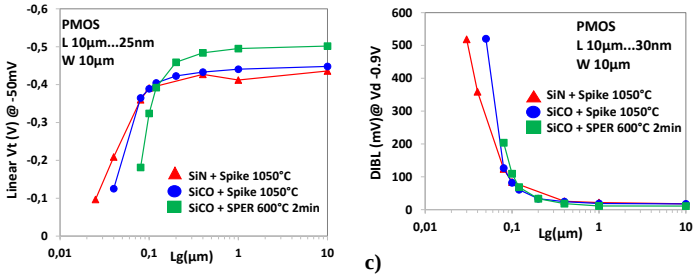


Fig.10: PMOS **a)** Ion/Ioff trade-off **b)** Linear Vt(L) **c)** DIBL(L) for HT anneal SiN and SiCO spacers and LT anneal SiCO spacer.

References : [1] P. Batude et al., IEEE Symposium on VLSI technology (2015) ; [2] C. Fenouillet-Beranger et al., IEEE Electron Devices Meeting (2014) ; [3] D. Benoit et al., IEEE Electron Devices Meeting (2015) ; [4] C.M.V-Lu et al., SSDM 2016 ; [5] L. Pasini et al., IEEE Symposium on VLSI technology (2015)