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RTA-Temperature Dependence of Electrical Characteristics of PVD-TiN Metal Gate SOI-MOSFETs Fabricated on Half-Inch Minimal Wafers

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Abstract

PVD-TiN metal gate MOSFETs and CMOS ring oscillators have successfully been fabricated by using gate-first process on half-inch minimal SOI wafers with different RTA-temperatures (T_R's), and the T_R dependence of their electrical characteristics have systematically been investigated. It was found that a positive shift of threshold voltage (V_t), a smaller V_t variation and an enhanced electron mobility are observed with reducing T_R. Moreover, the successful operation of a 561-stage CMOS ring oscillator with a gate length (L_g) of 0.36 μm has been demonstrated.

1. Introduction

The minimal-fab concept was proposed in the early 2008 for producing low volume custom devices with a low investment cost [1]. After the proposal of minimal-fab concept, many kinds of minimal-fab machines have been developed rapidly, as shown in Fig. 1. Meanwhile, the spin on dopant (SOD) thermal diffusion based gate-last process has also actively been promoted using the developed minimal-fab machines [2-4]. In this work, we develop gate-first process using the minimal-fab leaser heating machine combined with mega-fab ion implantation (I/I), and fabricate PVD-TiN gate MOSFETs and CMOS ring oscillators on the half-inch minimal SOI wafers with different RTA-temperatures (T_R's).

2. Device Fabrication

In the device fabrication, we used half-inch minimal SOI wafers, as shown in Fig. 2(a). First, thermal oxidation and device separation were performed to fabricate fully depleted (FD) SOI islands, as shown in Fig. 2 (b). Then, a 5.8-nm-thick gate oxide (T_{ox}) layer formation, a 30-nm-thick PVD-TiN and a 100-nm-thick TEOS-SiO_2 layers deposition were continually carried out. To fabricate submicron gate patterns using conventional minimal-fab maskless exposure machine, we introduced over-expose and O_2 plasma techniques, as shown in Figs. 2(c) and 2(d). Submicron gates were successfully fabricated by RIE of TEOS-SiO_2 layer and wet etching of PVD-TiN layer, as shown in Fig. 4(a). After the gate formation, BF_2^+ I/I for PMOS and P^+ I/I for NMOS were carried out separately using the same I/I conditions of dose = 1.5×10^{15} cm^{-2}, energy = 10 keV, tilt = 0°, and twist = 0°, as shown in Fig. 2(e). After a 145-nm-thick TEOS-SiO_2 layer deposition, RTA was performed with different T_R values but with the same time of 2 sec for different sample wafers using minimal-fab laser heating machine, as shown in Fig. 3. By using above I/I and RTA conditions, we also confirmed impurity activation with bulk Si wafers. Finally, conventional metallization and sintering were performed, as shown in Fig. 2(f). Figure 4(b) shows the photo-image of the process finished half-inch minimal SOI wafer that includes CMOS-TEG areas and 561-stage CMOS ring oscillators, and so on.

3. Electrical Characteristics

To investigate the T_R effect on electrical characteristics, we evaluated I_d-V_g characteristics of the fabricated MOSFETs with almost the same L_g of 3.37 μm on different sample wafers, as shown in Fig. 5(a). Note that almost the symmetrical I_d-V_g curve is observed in the MOSFETs on wafer-A. Figure 5(b) shows V_t as a function of T_R. It is clear that a positive V_t shift is observed with reducing T_R and the V_t values of the MOSFETs on wafer-A are close to those in the case of gate-last process without RTA [3, 4]. This result indicates that work function of PVD-TiN gate approaches to that of as deposited one with reducing T_R lower than 660 °C [5]. As a result, the CMOS inverter fabricated on wafer-A shows better transfer characteristics than others, as shown in Fig. 6. Moreover, the V_t roll-off in MOS and roll-up in PMOS are observed at a submicron gate region, as shown in Fig. 7. Such short channel effects (SCE) can be improved by introducing source-drain (SD) extension regions and the gate sidewall.

To investigate V_t variations, we evaluated 58-devices on etch sample wafer. As an example, Fig. 8 shows the I_d-V_g characteristics of the fabricated L_g of 0.25 and 1.27 μm NMOSFETs on wafer B, and the measured statistical V_t variations are shown in Fig. 9. Note that σV_t increases with scaling down device size owing to the large L_g fluctuation caused by submicron gate formation. Figure 10 compares the σV_t values of the fabricated MOSFETs with almost the same L_g of 1.27 μm on different sample wafers. It is clear that the smallest σV_t is observed in the fabricated MOSFETs on wafer A with the lowest T_R among three sample wafers.

To evaluate effective mobility, we also fabricated large size MOSFETs with L_g = 30 μm and W = 100 μm. It is clear from Fig. 11 that a higher drain current, a large capacitance and an enhanced electron mobility are observed in the NMOSFET on wafer-A than those on wafer-C. The performance degradation in the MOSFETs on wafer-C should be resulted from the nitrogen atoms pile-up near the channel surface in T_{ox} layer due to the high T_R [5]. Figure 12 shows the oscillation wave form of the fabricated 561-stage CMOS ring oscillator with L_g = 0.36 μm. This result means that submicron gate 1122-transistors are operated simultaneously.

4. Conclusions

We have fabricated and characterized PVD-TiN gate SOI-MOSFETs with different T_R values. It was found that T_R of 660 °C is suitable for the fabrication of PVD-TiN gate CMOS, and the higher T_R than 660 °C results in device performance degradation. Moreover, the successful operation of a 561-stege CMOS ring oscillator has been demonstrated. This indicates that CMOS integrated circuits can be fabricated using the developed gate-first minimal-fab process.

References

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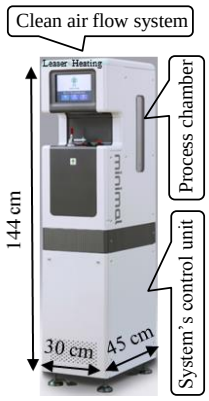


Fig. 1. Photo-image of the developed minimal-fab machine.

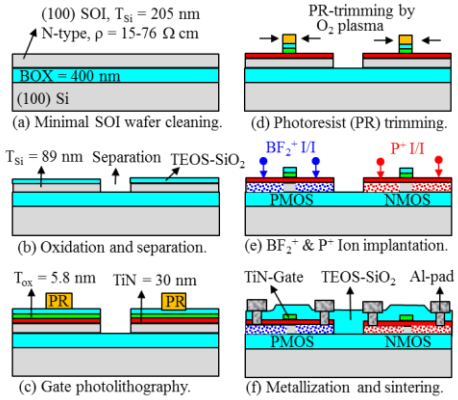


Fig. 2. Ion implantation (I/I) based gate-first device fabrication process flow for the PVD-TiN metal gate SOI-CMOS.

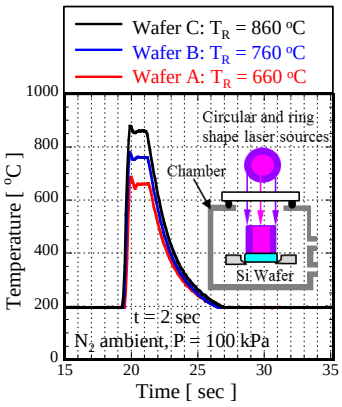


Fig. 3. RTA-temperature (T_R) profiles of the wafers by using minimal-fab laser heating.

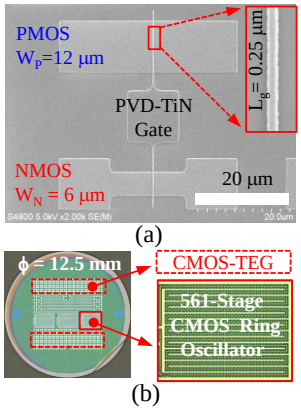


Fig. 4. (a) SEM of CMOS pattern after TiN gate formation, and (b) photo-image of minimal wafer.

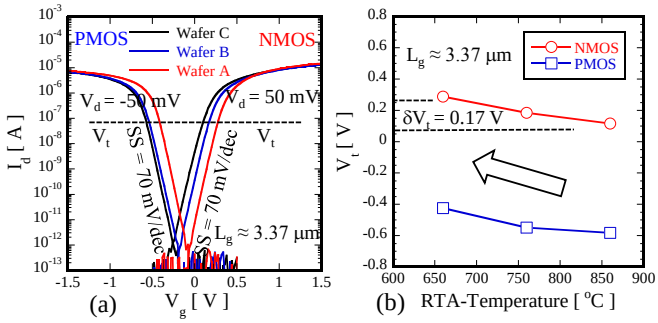


Fig. 5. (a) I_d-V_g characteristics of the fabricated SOI-MOSFETs with almost the same L_g of 3.37 μm on the different sample wafers, and (b) T_R dependence of the threshold voltage (V_t).

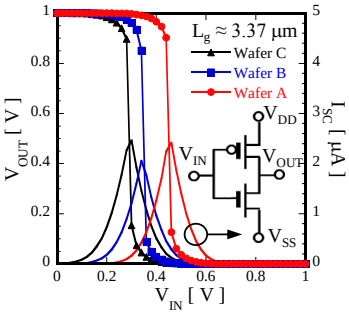


Fig. 6. Transfer characteristics of the fabricated CMOS inverters on the different sample wafers.

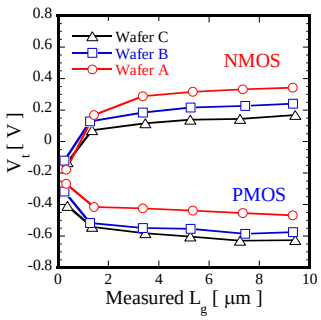


Fig. 7. V_t as a function of L_g for the fabricated SOI-MOSFETs on the different sample wafers.

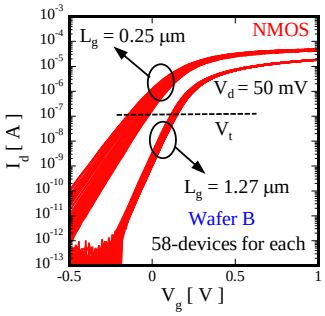


Fig. 8. I_d-V_g characteristics of the fabricated NMOSFETs with different L_g values of 0.25 and 1.27 μm.

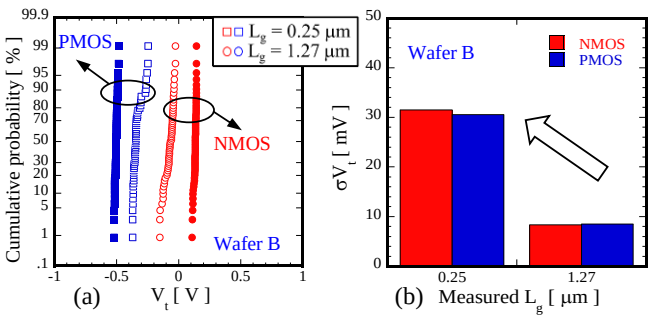


Fig. 9. (a) Statistical V_t variations and (b) σV_t values of the fabricated MOSFETs with different L_g values of 0.25 and 1.27 μm. σV_t increases with scaling down L_g.

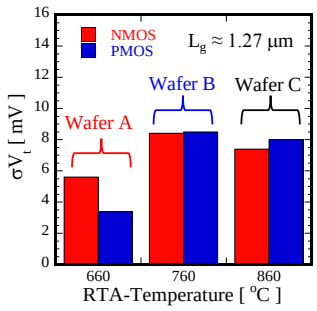
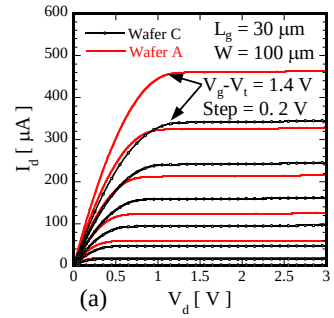
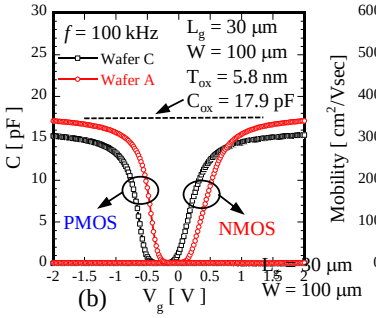


Fig. 10. Comparison of the σV_t of the fabricated SOI-MOSFETs with different T_R values.





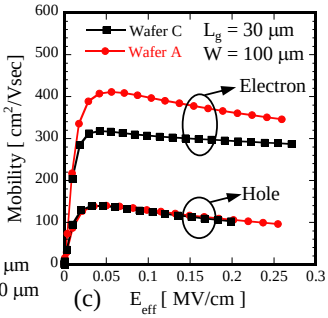


Fig. 11. Comparison of electrical characteristics between the fabricated large size MOSFETs on wafer-A and wafer-C. (a) I_d-V_d characteristics of NMOSFETs at the same V_g-V_t, (b) split C-V characteristics, and (c) effective mobility. Electron mobility enhancement is observed in the NMOSFET on wafer-A.

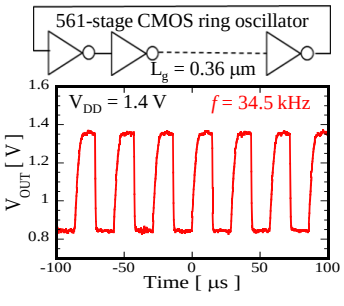


Fig. 12. Oscillation wave form of the fabricated 561-stage CMOS ring oscillator.