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Influence of Material Parameters on the Performance of Accumulation Mode DRAM

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Abstract

The work proposes an Accumulation Mode capacitorless 1T DRAM and analyzes key metrics, retention time, sense margin, speed, and power, and associated trade-offs. New viewpoints highlight the advantages, challenges and dominating parameters for different semiconducting materials (Silicon and Germanium) for application specific design.

1. Introduction

The increase in demand for high speed memory [1] requires downscaling of MOSFETs which is limited by short channel effects and fabrication of ultra-sharp junctions [2]. The problem can be overcome by the use of Accumulation Mode (AM) devices that have the same type of dopants in source/drain and channel [2]. The work presents a study of material parameters and their impact on (i) Retention Time (*RT*), which estimates refresh cycles, (ii) Sense Margin (*SM*), which determines the read sensitivity, (iii) Write Time (*WT*) that governs speed, and (iv) Write bias (V_{D_W1}) that governs the power consumed. As these metrics indicate trade-offs, balance between them requires a careful investigation which is made feasible through an analysis of key material parameters. The optimal material-device co-design would be beneficial for IoT, mobile, networking and cloud computing applications where the focus is on low power, increased storage density, retention and speed.

2. Results and Discussion

AM device with channel doping (N_d) of 10^{18} cm^{-3}, gate length (L_g) of 100 nm, film thickness (T_{Si} or T_{Ge}) of 10 nm, gate oxide thickness (T_{ox}) of 1 nm (SiO_2 for Silicon (Si) and GeON for Germanium (Ge)) with 10 nm underlap (L_{un}) were analyzed using ATLAS tool [3] with well calibrated models against published experimental data [4] shown in Fig. 1. The base value of carrier lifetime (τ_0) for Si and Ge was considered to be 100 ns and 1 µs, respectively, at 27 °C, for doping of 10^{15} cm^{-3}, and its degradation with doping and temperature was included in the analysis [5-9]. Fig. 2(a) shows the schematic of AM device. The drain current (I_d) – gate voltage (V_G) characteristics for the same is shown in Fig. 2(b). The functionality as DRAM requires deeper potential well (storage region) and an independent gate operation [6-9], with front gate (G1) used for conduction and back gate (G2) for charge storage. DRAM operation, based on the distribution of holes in storage region, is schematically represented in Figs. 3(a)-(c) for state "1" and Figs. 3(d)-(f) for state "0" for Write (W), Hold (H) and Read (R) operations, respectively.

Write "1" operation (Fig. 3(a)) is performed through Band-to-Band-Tunneling (BTBT) at G2 and drain junction with a bias of 1.0 V at G1, 1.5 V at drain and -1.5 V at G2. Write "0" operation (Fig. 3(d)) is performed through forward bias mechanism with bias of 1.5 V at G1 and G2. Presence of holes in the storage region indicates higher current due to barrier lowering at the front surface (Fig. 3(c)), while absence of holes increases the barrier, and consequently reduces the read current (Fig. 3(f)). The difference between read currents (I_1-I_0) is termed as *SM*, while *RT* is the time when maximum *SM* reduces by 50% [6-9]. State "1" is disturbed by thermal Recombination (REC) and diffusion of holes during Hold "1" from the potential well as shown in Fig. 3(b) while state "0" is perturbed by the accumulation of holes in the potential well due to thermal Generation (GEN) and BTBT during Hold "0" as shown in Fig. 3(e) [6-9]. Fig. 4 reflects the same while comparing band energy profiles of Si and Ge devices, where the variation in bandgap (E_g) and barrier height (ΔE_b) influence GEN and REC.

A lower ΔE_b represents a shallower potential well that affects hole sustenance, while a lower E_g indicates higher BTBT. Other than E_g and ΔE_b, DRAM metrics can be optimized through carrier lifetime (τ_0), which along with being material property, is also influenced by temperature and doping. For fixed N_d (= 10^{18} cm^{-3}), the reduction in the temperature dependent lifetime (τ) increases hole recombination during Hold "1", and thus, degrades *RT* (Fig. 5) for Si. Thermal GEN increases with temperature (Fig. 2(b)) and degrades state "0", and the retention. Maximum *RT* achieved is 150 ms at 27 °C, and 12 ms at 125 °C. Even a higher carrier lifetime (1 µs at 27 °C for doping of 10^{15} cm^{-3}) for Ge could not assist in retaining the states due to lower E_g and higher mobility.

The purpose of W1 is to speed up accumulation of holes in the storage region, and the same is governed by Write Time (*WT*) and drain bias (V_{D_W1}) which help in estimating speed and power consumption, respectively. As *SM* is based on the hole concentration during read, which decreases from W1 to H1 to R1 (Figs. 3(a)-(c)), the time and bias for W1 is estimated as the time when *SM* attains a constant value [8]. The reduction in recombination rate due to higher carrier lifetime preserves more holes in the body during R1, which increases current for R1, and thus, *SM* attains a constant value at lower (a) *WT* for fixed V_{D_W1} and (b) V_{D_W1} for fixed *WT*. For a fixed *WT* = 35 ns, V_{D_W1} can be reduced from 1.5 V to 0.9 V if τ_0 can be increased (10^{-8} s to 10^{-6} s). Similarly, for a fixed V_{D_W1} of 1.5 V, *WT* reduces for the same range of τ_0 (Fig. 6). *RT* increases with τ_0 (from 10 ns to 1µs) due to longer sustenance of holes in the potential well during H1 as recombination of holes is reduced. Further, increase in τ_0 marginally affects recombination in the potential well and results in a lower increase in *RT* (> 1 µs).

Materials with higher τ_0 such as Ge requires less write time (*WT* = 10 ns) as well as lower drain bias (V_{D_W1} = 0.3 V) with different biasing scheme as compared to Si based DRAM due to higher BTBT, influenced by low E_g, higher mobility. Thus, although Ge has high τ_0, these parameters reduces *RT*. Higher mobility in Ge degrades state "1" due to diffusion while lower E_g degrades state "0" due to GEN and BTBT. Fig. 7 shows the variation in *RT* with carrier lifetime with gate length of 100 nm for Ge. The maximum *RT* achieved for the optimized bias for Ge is 5 ms and 3 ms at 27 °C and 85 °C, respectively. Fig. 8 compares DRAM metrics (*SM*, *RT*, *WT*, V_{D_W1} and *Power*) for Si and Ge, and shows the benefits in terms of low V_{D_W1} and increased write speed for Ge. However, the factor that reduces *RT* in Ge is E_g [10]. Due to higher BTBT, Ge DRAM is expected to exhibit a higher current for W1 at a lower drain bias, which results in nearly the same power consumption (~55 nW/µm). Factors influencing *RT* of memory are temperature, τ_0 and E_g. Therefore, from a material viewpoint, Fig. 9 suggests that although τ_0 for Ge is more than Si, retention achieved is lower. Also, comparing Si with GaAs shows higher E_g for

GaAs, but possibly a lower retention due to reduced carrier lifetime that increases REC. The analysis highlights the need for proper material system engineering to provide additional degree of freedom to enhance DRAM metrics and regulate REC and GEN through optimal values of τ_0 and E_g.

3. Conclusion

The work demonstrates the impact of temperature, carrier lifetime and bandgap of Si and Ge AM transistors on capacitorless DRAM. Si DRAM shows better performance due to combination of lower mobility and higher bandgap despite a lower lifetime in comparison to Ge. The analysis of trade-offs reflects on the choice of appropriate material in emerging technologies for IoT, mobile, networking and cloud computing applications.

Acknowledgements

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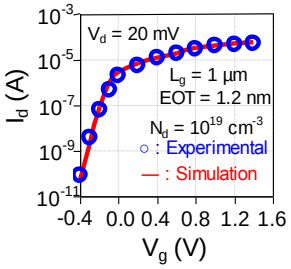

Fig. 1 Comparison of transfer characteristics (I_d-V_G) of single gate JL MOSFET with experimental data [4].

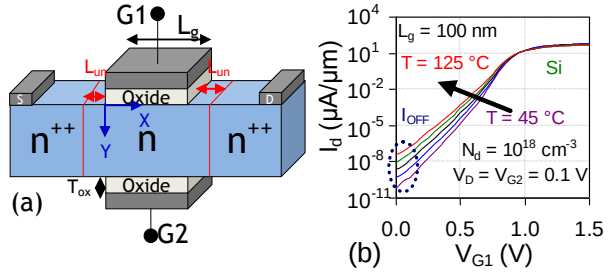

Fig. 2 (a) Schematic diagram of Double Gate (DG) Accumulation Mode (AM) MOSFET. (b) I_d-V_G characteristics of Si AM device at different temperatures. I_{OFF} indicates the off current at (V_{G1} = 0 V).

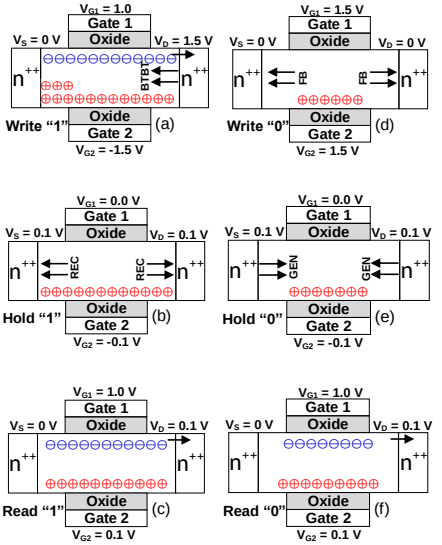

Fig. 3 Operation of AM as a 1T DRAM with (a) Write "1" for 35 ns, (b) Hold "1", (c) Read "1" for 100 ns, (d) Write "0" for 35 ns, (e) Hold "0" and (f) Read "0" for 100 ns. Various mechanisms in the devices are Band-To-Band-Tunneling (BTBT), Recombination (REC), Forward Bias (FB) and Generation (GEN).

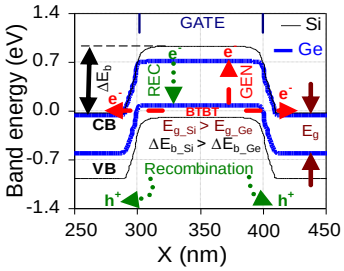

Fig. 4 Band energy profile for Si and Ge at zero applied bias. Conduction Band (CB), Valence Band (VB), Bandgap (E_g) and Barrier height (ΔE_b) are shown.

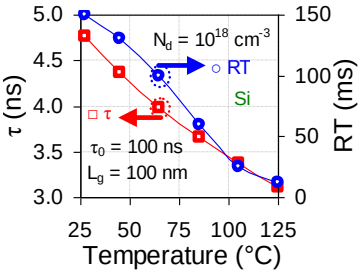

Fig. 5 Variation of carrier lifetime (τ) and RT with temperature for $N_d = 10^{18}$ cm^{-3}. τ_0 of 100 ns and 1 µs are the default lifetime values at 27 °C for Si and Ge, respectively.

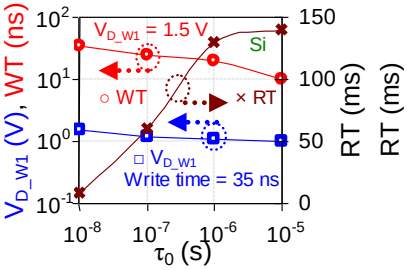

Fig. 6 Variation in write drain bias (V_{D_W1}) at fixed write time (WT) = 35 ns and WT at fixed V_{D_W1} = 1.5 V, and RT with τ_0 at 27 °C for Si.

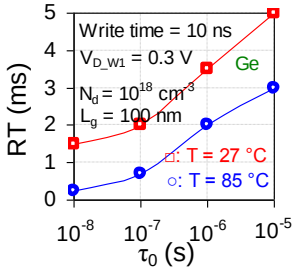

Fig. 7 Variation in RT with τ_0 at 27 °C and 85 °C DRAM with L_g of 100 nm for Ge.

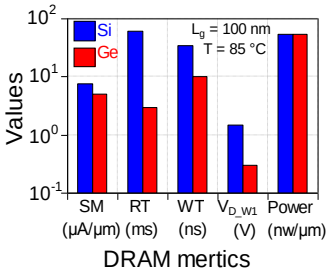

Fig. 8 Comparison of Si and Ge in terms of DRAM metrics for L_g = 100 nm at 85 °C.

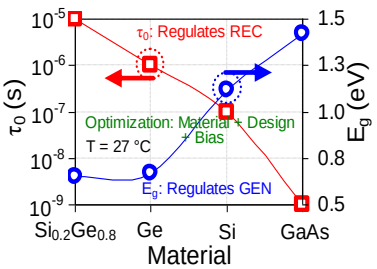

Fig. 9 Variation in lifetime (τ_0) and bandgap (E_g) for different materials at 27 °C.