

Vertical Double-Gate 1T DRAM with an Asymmetric Oxide Barrier for Significant Enhancement of Data Retention

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Abstract

In this work, a 1-transistor dynamic random access memory (1T DRAM) in a novel structure with vertical double gates and asymmetric oxide barrier is proposed and designed by technology computer-aided design (TCAD) simulation. The double gates are independently operated and consist of sensing gate (SG) for read operation and control gate (CG) for write/erase operations. The proposed 1T DRAM cell demonstrates a notably high sensing margin $\sim 10^9$ between 1 and 0 states and significantly enhanced retention time of 600 ms, which mainly attribute to the high gate controllability over the channel by double-gate operation and the effective hole confinement by asymmetric oxide barrier, respectively.

1. Introduction

Conventional DRAM unit cell has 1 transistor and 1 capacitor for switching and charge storage. Large capacitance is required for storing larger amount of charges in order for better data discrimination. However, the capacitor has been regarded as the hindrance in pursuing the extreme device scaling in the DRAM technology. A practically high capacitance near 30 fF/cell is achieved in recent days by capacitors in either stack or deep-trench structure in the embedded DRAM [1], the process architecture is highly complicated and the yield issues might remain unquenched. Efforts have been dedicated for truncating the capacitor towards more system-on-chip (SoC) oriented DRAM technology with higher integration density [2–5]. For write operation of 1T DRAM, impact ionization has been adopted to accumulate the mobile holes in the floating body [6]. It is found in more recent literature that band-to-band tunneling can be also employed for writing mechanism in the scaled devices [7]. The generated carriers defining a new data state vanish mostly through recombination and drift/diffusion. In order to enhance retention time, a physical blockage embracing the floating body by dielectric can be schemed [8]. However, significant amount of holes with less proximity to the gate remain at the bottom of floating body even after an erase operation, which makes the sensing margin between 1 and 0 states undesirably small.

In this work, a vertical double-gate (VDG) 1T DRAM is proposed, designed, and characterized. The write operation is performed by band-to-band tunneling for lower power consumption and higher applicability to scaled devices. Double-gate device operation featuring an asymmetric oxide barrier greatly enhances the data discrimination and retention.

2. Device Structure and Simulation Strategy

Fig. 1(a) and (b) show the schematics of single-gate/symmetric oxide barrier and double-gate/asymmetric oxide barrier 1T DRAM cells, respectively. The proposed VDG 1T DRAM in Fig. 1(b) has two independent gates, sensing gate (SG) for read operation and control gate (CG) for write/erase operations. In the simulation, vertical Si channel length (L_{Si}) and thickness (T_{Si}) are 200 nm and 15 nm, respectively. The length (L_{ox}) and thickness (T_{ox}) of barrier oxide are 14 nm and 1 nm, respectively. The equivalent oxide thickness of the gate dielectric is 3 nm. The doping concentrations for source, channel, and drain junctions are n -type $10^{20}/\text{cm}^3$, p -type $10^{18}/\text{cm}^3$, and n -type $10^{20}/\text{cm}^3$, in sequence.

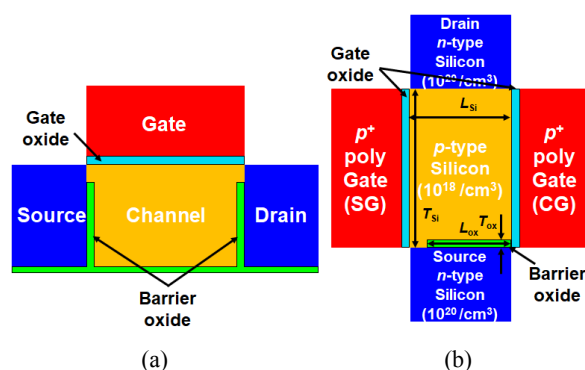


Fig. 1 Schematics of (a) single-gate/symmetric oxide barrier and (b) vertical double-gate/asymmetric oxide barrier 1T DRAM cells.

For higher reliability in simulation results, multiple models including concentration-dependent mobility model, concentration-dependent generation-recombination model, bandgap narrowing model, and Fermi-Dirac statistics model were simultaneously activated. Further, non-local inter-band tunneling calculation was applied for even higher accuracy.

3. Results and Discussion

Write and erase operations are realized by band-to-band tunneling and drift/diffusion, respectively, mainly by the p^+ poly-Si CG. Fig. 2(a) and (b) show the energy-band diagrams for write (along the cutline A-A') and hold (along the cutline B-B') operations, respectively. Under a write operation condition, $V_{CG} = -0.5$ V and $V_{DS} = 1.5$ V, the energy-band shows a steep bending as shown in Fig. 2(a) and the valence electrons in the p -type channel tunnel into the n^+ drain junction. The newly generated holes remain in the p -type channel, floating body, and the memory state is changed from 0 to 1.

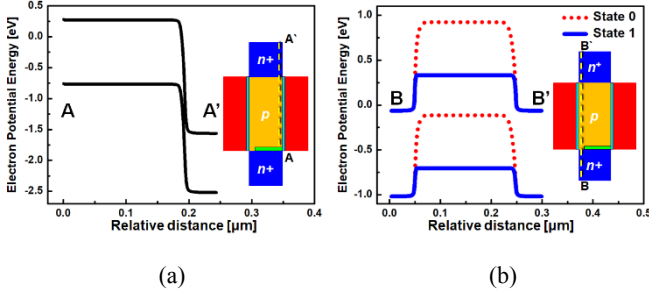


Fig. 2 Energy-band diagrams (a) under write operation condition (along the cutline A-A') and (b) for state 0 and 1 (cutline B-B').

After a program operation, the unpaired holes are accumulated in the floating body leading to state 1, which elevates the body potential and lowers the bands as shown in Fig. 2(b).

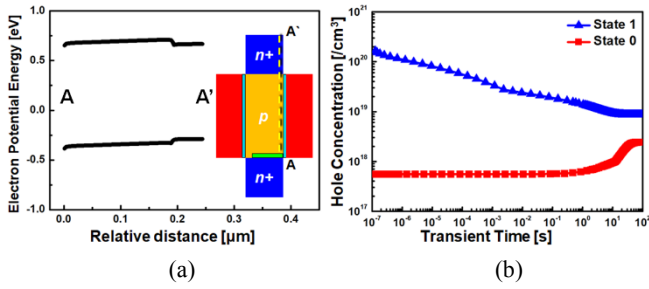


Fig. 3 Erase operation. (a) Energy-band diagram under the erase operation condition (along the cutline A-A'). (b) Changes of hole concentrations at state 1 and 0 as a function of transient time.

Fig. 3(a) shows the energy-band diagram under an erase operation condition, $V_{CG} = 0.5$ V and $V_{DS} = -0.7$ V. The negative V_{DS} gets rid of the channel-to-drain hole potential barrier and the holes accumulated in the floating body are swept out to drain junction by drift and diffusion, leading back to state 0. Fig. 3(b) depicts the hole concentrations at state 1 and 0 as a function of time, with no bias, after write 1 and 0 operations. It is confirmed that the decay of stored holes is relatively faster but the decade change requires a rather long time > 1 s.

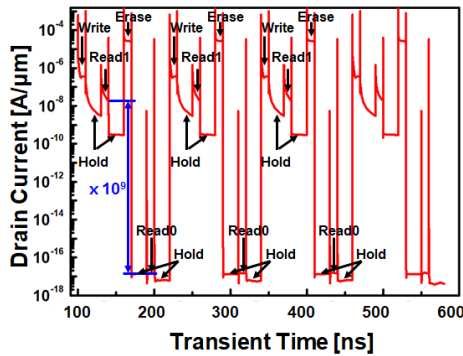


Fig. 4 4-cycle memory operation of the VDG 1T DRAM.

Fig. 4 shows the sensing margin over the 4-cycle memory operation where one cycle consists of 8 steps: write 1/hold/read 1/hold/write 0 (erase)/hold/read 0/hold. The ratio between read-1 and read-0 currents is maintained to be about 10^9 being invariant with number of cycles and time. Although

there are hold operations among write, erase, and read operations, there is no energy consumption for hold, since it is assumed that there is no bias applied to the device terminals.

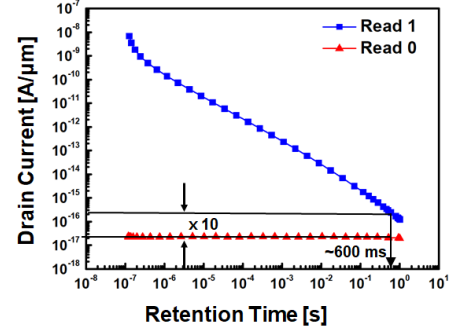


Fig. 5 Retention: read-1/read-0 currents as a function of time.

Fig. 5 confirms that the retention time reaches 600 ms for a presumable reference of read-1/read-0 current ratio of 10, which mainly attributes to the asymmetric oxide barrier effectively preventing the drift and diffusion of body holes. Table I summarizes the possible operation voltage scheme and the energies required for individual operations. It is revealed that write 0 operation has the largest portion since the write 0 current is the highest one as was shown in Fig. 4, owing to both source-to-drain electron and body-to-drain hole currents.

Table I Possible operation voltage scheme (10-ns operation assumed)

	V_{SG} [V]	V_{CG} [V]	V_{DS} [V]	Time [ns]	Energy [J]
Write 1	0	-0.5	1.5	10	5.25×10^{-7}
Write 0	0.5	0.5	-0.7	10	5.20×10^{-6}
Read 1	0.2	0.2	0.2	10	1.40×10^{-8}
Read 0	0.2	0.2	0.2	10	1.05×10^{-17}
Hold	0	0	0	20	0

4. Conclusion

In this work, a VDG 1T DRAM with an asymmetric oxide barrier has been proposed, designed, and characterized. High integration density and low-power operation capability are expected by the merits by VDG structure and operation mechanisms. The asymmetric oxide barrier increases retention time by physically blocking the leakage by drift-diffusion of stored holes. The VDG 1T DRAM is regarded to be a highly promising component in the advanced DRAM technologies.

Acknowledgements

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