Extended Abstracts of the 2018 International Conference on Solid State Devices and Materials, Tokyo, 2018, pp153-154

First Implementation of MONOS Flash Memory in SOTB-CMOS

Keiichi Maekawa, Yuto Omizu, Hideki Makiyama, Yoshiki Yamamoto, Hideaki Yamakoshi, Kenichiro Sonoda, Hiroshi Yanagita, Hiroki Shinkawata, Takashi Hashimoto, Yasuo Yamaguchi, and Tomohiro Yamashita

Renesas Electronics Corporation, 751 Horiguchi, Hitachinaka, Ibaraki, 312-8504, Japan
TEL: +81-29-270-3111, E-mail: keiichi.maekawa.fn@renesas.com

Abstract

MONOS (Metal Oxide Nitride Oxide Semiconductor) flash memories have been fabricated on SOI substrate with SOTB (Silicon on Thin Box) structure, and their memory characteristics and reliability have been investigated for the first time. The SOTB-MONOS with channel dopant-less structure was confirmed that threshold voltage (Vth) variability after program and erase (P/E) operation improved by about 30% with comparable operation speed and reliability as conventional MONOS fabricated on a bulk wafer (Bulk-MONOS). In the case of SOTB-MONOS, it is found that some unselected bits of cell array may fall into the weak erase state during program operation because the potential of the Si-body, which is isolated from the substrate by the BOX layer, is floating. It is shown that this disturbance can be suppressed by inserting a short time reset sequence during program operation.

1. Introduction

MONOS cell with charge trap ONO film has good affinity with conventional CMOS process and power consumption can be suppressed because P/E operation is performed by Fowler-Nordheim (FN) tunneling [1,2]. The Vth variability after P/E operation is one of important parameters for memory reliability margin in MONOS cell array. Since the random Vth variation in MOSFET is proportional to the gate dielectric film thickness [3], the Vth variability in the memory cell having the rather thick ONO film will be larger than that of the core device. Vth variability in SOTB MOSFETs, which has FDSOI structure, is much smaller than bulk MOSFETs because of channel dopant less structure [4], which makes SOTB a powerful solution for low voltage operation of peripheral circuits. However, there are few reports about not only the memory characteristics but also the Vth variability about MONOS flash memories fabricated on FDSOI. In this paper, we investigate on the memory characteristics of MONOS flash memories fabricated on SOTB (SOTB-MONOS) as compared with ones fabricated on the conventional bulk wafer (Bulk-MONOS).

2. Experiment

The SOTB-MONOS process is added on the 65nm-node SOTB-CMOS process. The ONO stack structure is compatible with Bulk-MONOS. Figure 1 shows typical cross-sectional TEM image of SOTB-MONOS. In this work, the SOTB-MONOS is composed of the control gate (CG) of the memory and the select gate (SG) of the switch MOS which are connected in series. Each gate width and length of CG and SG are 0.1x um. The parallel and decoder type TEG is used for memory cell characterization and the Vth variation assessment, respectively.

3. Results and Discussion

The program and erase operations are performed by FN tunneling. Table 1 shows an example of memory cell voltage configuration. Figures 2-4 show the typical P/E characteristics, data retention, and P/E cycle characteristics. Under the same voltage, the operation speed and reliability of SOTB-MONOS were almost comparable to that of Bulk-MONOS. Figure 5 shows the hole distribution during the erase operation in SOTB-MONOS by device simulation. BTBT (Band to Band Tunneling) induced holes are accumulated in the Si-body, which is isolated by BOX layer. During the erase operation of 1ms, the holes were accumulated over $1x10^{20}$ cm^{-3} under the center of the memory gate, and this amount is sufficient for erase operation. Figure 6 shows Pelgrom plot of Vth variation after program operation. It was improved about 30% in SOTB-MONOS as compared to that in Bulk-MONOS. This tendency was also seen for the erase operation. These results mean that data-retention life time of worst bit in case of 1Mbit cell array are extended by ten times or more by Vth variation decrease as shown in fig.7.

Figure 8 shows an example of program operation in cell array. In the case of SOTB-MONOS, the weak erase state is gradually generated in the unselected bit region C (Us-C) because the potential of Si-body is in the floating state due to the existence of BOX layer. Figure 9 shows the tendency curves of the hole concentration in Si-body by using device simulation. There was a transition period of a few micro sec before the Us-C falls into the weak erase state. Figure 10 (a) and (b) show the simulated waveforms of the electric field in the ONO film and the carrier concentration in Si body at the weak erase state, respectively. The electric field gradually enhances because holes are accumulated in Si-body by BTBT. But it is found that this electric field can be half or less by periodically inserting reset sequence in which the word and bit line are equipotential during program operation. Figure 11 shows the weak erase characteristics of the Us-C during program operation. It was confirmed that this disturbance in SOTB-MONOS was almost same as compared to Bulk-MONOS by inserting the reset sequence with micro sec order because the transiently generated holes disappeared due to recombination with induced electrons by reset sequence as shown in fig.10 (b).

4. Conclusions

The MONOS with SOTB technology have been fabricated. Vth variability at P/E operation improves by about 30% with operation speed and reliability compatible as compared to Bulk-MONOS. Disturbance in unselected bits due to the existence of BOX layer is optimized by inserting the short time reset sequence in program operation.

References

[1] H. Mitani, et al., ISSCC2016, 7.6, pp140-142.
[2] K. Ramkumar, et al., IMW2013, pp190-192.
[3] N. Sugii, et al., IEEE TED, vol.57, No.4, April 2010.
[4] Y. Yamamoto, et al., 2012VLSI Tech., T109.

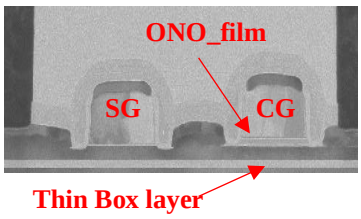

Fig. 1. Cross-sectional TEM image of SOTB-MONOS.

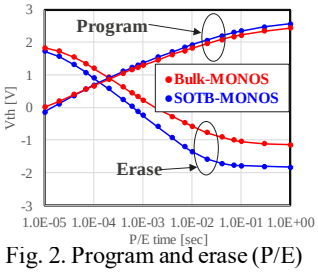

Fig. 2. Program and erase (P/E) characteristics in Bulk- and SOTB-MONOS. Temp.=25°C

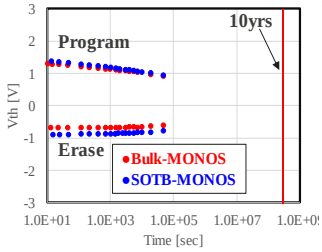

Fig. 3. Data retention characteristics in Bulk- and SOTB-MONOS after 10k cycle. Temp.=85°C

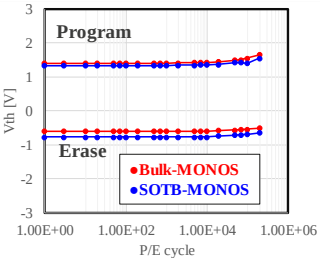

Fig. 4. P/E cycle characteristics in Bulk- and SOTB-MONOS. Temp.=85°C

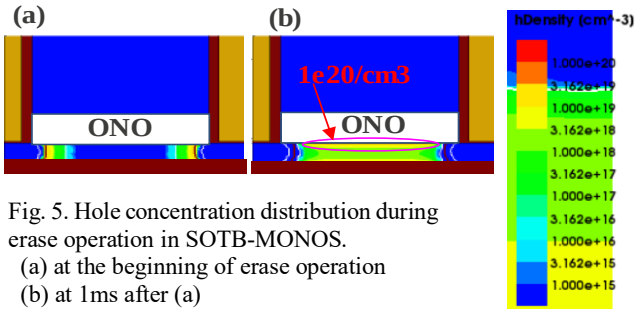

Fig. 5. Hole concentration distribution during erase operation in SOTB-MONOS.
(a) at the beginning of erase operation
(b) at 1ms after (a)

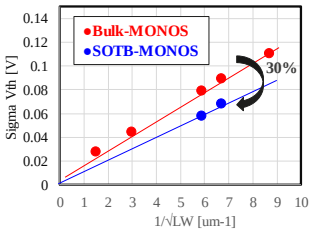

Fig. 6. Vth variation after program operation in conventional and SOTB-MONOS.

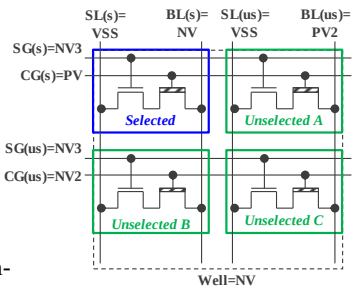

Fig. 8. An example of program operation in cell array.
PV : Positive Voltage,
NV : Negative Voltage,
SG : Select Gate,
CG : Control Gate,
SL : Source Line
BL : Bit Line,
(s) : Select Line,
(us) : Unselect Line
PV>PV2>0V
NV<NV2<NV3<0V

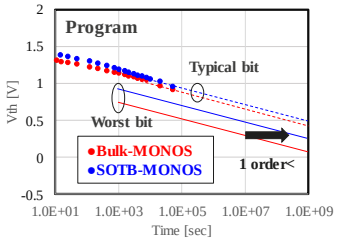

Fig. 7. The prediction of data retention characteristics in worst bit after 10k cycles. Temp.=85°C

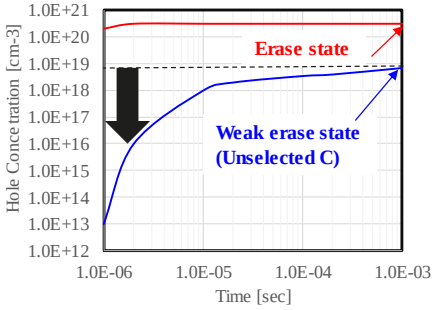

Fig. 9. Tendency curves of the hole concentration in Si-body by using device simulation.

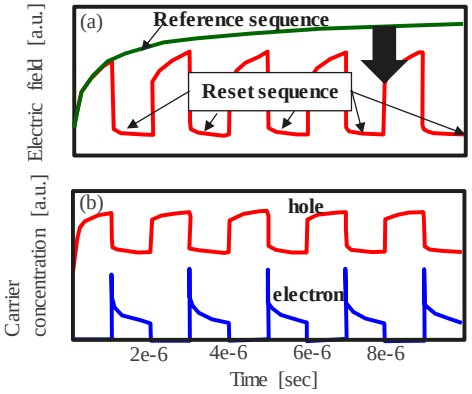

Fig. 10. Simulated waveforms of (a) the electric field in the ONO film and (b) the carrier concentration in Si body at the reference and reset sequence. The word line and bit line in reset sequence are equipotential.

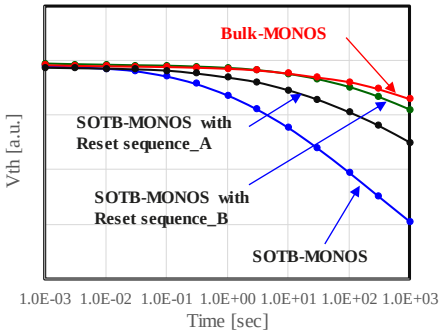

Fig. 11. Weak erase characteristics of the Us-C during program operation.
Sequence A : interval time = 10 usec
Sequence B : interval time = 2 usec

Operation	CG	SG	BL	SL	WELL
Program	PV	Vss	NV	Vss	NV
Erase	NV	Vcc	PV	Vss	PV

Table. 1. An example of memory cell voltage configuration.
PV : Positive Voltage
NV : Negative Voltage