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Gate-All-Around Transistors Based on Vertically Stacked Si Nanowires: Recent Progress in CMOS Integration and in Advanced Inline Metrology

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Abstract

We report on vertically stacked gate-all-around Si MOSFETs for CMOS scaling beyond FinFET technology. Process challenges, circuit demonstration, and advanced inline metrology, including nanowire scatterometry and SEM-based contact inspections, are discussed in relation to recent research results.

1. Introduction

Gate-All-Around (GAA) field-effect transistors offer optimal electrostatic control over nanowires/sheets, which enables downscaling of the gate length to below the FinFET limit, while maintaining low off-state leakage. Therefore, GAA devices are promising candidates to replace FinFETs in future CMOS nodes [1,2]. In the context of this potential scaling pathway, we will discuss recent progress in CMOS integration and in advanced inline metrology of Si GAA devices.

2. GAA device fabrication

Si GAA devices were fabricated starting from ground plane (GP) ion implantation (**Fig. 1a**), SiGe/Si epitaxy (**Fig. 1b**), and fin/STI formation (**Fig. 1c**) [3-5]. After that, dummy gates and spacers were defined, before the SiGe/Si fins in the source/drain (S/D) regions were replaced by embedded S/D epi (**Fig. 1d**) [5]. The Si channels were then released in the replacement metal gate (RMG) module by selective removal of the SiGe sacrificial layers (**Fig. 1e**) before high-k/metal gate formation **(Fig. 1f**). Based on this process flow, both rounded nanowires (**Fig. 2a**) and nanosheets (**Fig. 2b**) have been demonstrated for different release processes [3,5].

3. CMOS integration

Independent threshold voltage control for N- and PMOS Si GAA devices has been demonstrated by dual work function metal (DWFM) integration (**Fig. 3**) [4]. The N/P boundary can be recognized by the discontinuity at the gate trench sidewalls in top-view SEM images taken after pMetal etch, before nMetal deposition (**Fig. 3a**). Cross-sectional TEM images of the final devices show the different metals wrapping around the P- and NMOS nanowires (**Fig. 3b – d**).

The subthreshold slope (*SS*) for NMOS GAA devices and reference FinFETs is shown in **Fig 4a**: *SS* degrades at short L_G for GAA devices with low GP doping, similar to FinFETs with comparable junctions. In contrast, good *SS* (65mV/dec.) at short L_G is maintained for GAA devices with sufficiently high GP doping. The I_S-V_{GS} characteristics for L_G = 24 nm (**Fig. 4a inset**) indicate that the *SS* improvement by high GP doping can be attributed to suppression of punch through in the parasitic channel below the nanowires [3]. Similar trends are observed for PMOS GAA devices (**Fig. 4b**): Sufficiently high GP doping is required to maintain good *SS* at short L_G.

Integration of N- and PMOS GAA devices with matched V_T on the same wafer (**Fig. 5**) has paved the way towards ring oscillator (RO) demonstration based on stacked Si GAA devices [5]. The reduction in gate delay with increasing V_{DD} and with decreasing L_G (**Fig. 6**) confirms proper RO functionality. For further AC performance optimization, parasitic capacitance reduction by inner spacers is essential [1,2]. The integration of these device elements is a key process challenge for GAA. Proof-of-concept inner spacer integration by cavity etch and dielectric fill/etchback are illustrated schematically in **Fig. 7a** and by TEM in **Fig. 7b** [5].

4. Advanced inline metrology

The complex three-dimensional geometry of GAA devices puts new challenges to inline metrology. Scatterometry, also known as Optical Critical Dimension (OCD), enables structural characterization of Si GAA devices by 3D modeling of light scattering from arrays of devices (**Fig. 8**) [6]. For example, nanowire CD can be extracted by this methodology in a fast and non-destructive way and in agreement with TEM results (**Fig. 9, 10**) [6]. At the same time, OCD provides a full set of additional structural output parameters.

Another advanced inline metrology example is voltage-contrast SEM imaging (**Fig. 11**) [7]. This method enables inline detection (based on nanowire charging) of top-nanowire contact issues (**Fig. 12**). Further refinement of this method provides a route towards inline estimation of nanowire parasitic resistance and capacitance [7].

5. Conclusions

Recent results on CMOS integration and advanced inline metrology of Si GAA devices demonstrate the progress in GAA CMOS technology development.

Acknowledgements

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References

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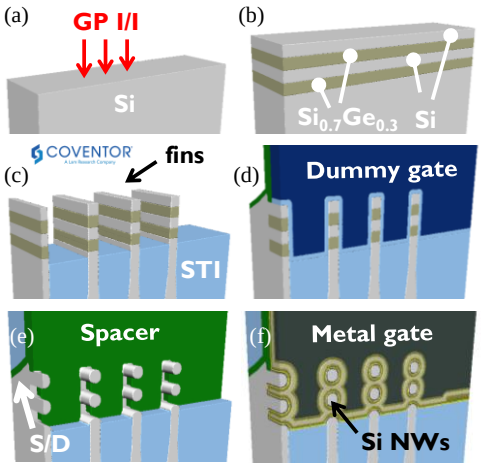

Fig. 1. Si GAA fabrication (Coventor® images). After SiGe/Si fin formation (a) – (c), the Si channels are released by selective SiGe removal in the replacement metal gate module (d) – (f).

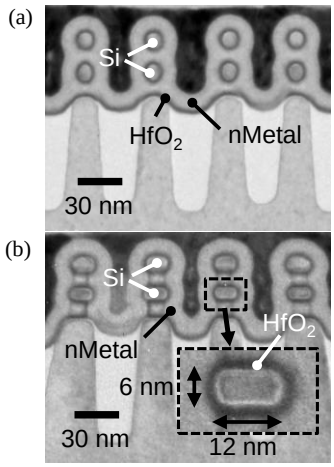

Fig. 2. (a) Rounded Si nanowires with a diameter of 8 nm, and (b) Si nanosheets with a thickness of 6 nm and a width of 12 nm.

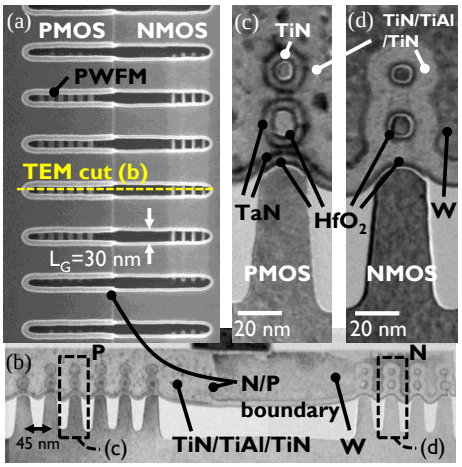

Fig. 3. Dual work function metal integration. (a) Top-view SEM image after pMetal etch from the NFETs, and (b) – (d) cross-sectional TEM images of P- and NFETs at the end of process.

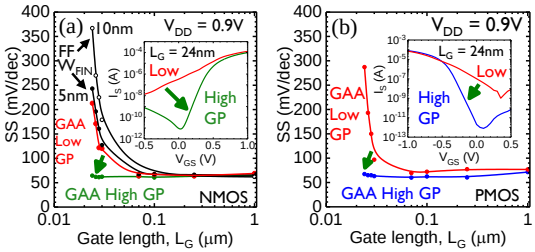

Fig. 4. SS_{SAT} vs. L_G for (a) NMOS and (b) PMOS, showing improved GAA device electrostatics for GP configurations that suppress the bottom parasitic channel. **Insets**: Punch through is prevented by GP doping.

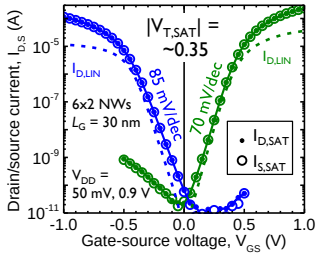

Fig. 5. $I_{D,S}$-V_{GS} for PMOS and NMOS with matched V_T by DWFM integration.

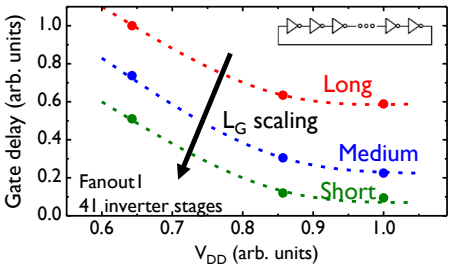

Fig. 6. Ring oscillator gate delay vs. V_{DD}. Gate delay reduces with increasing V_{DD} and decreasing L_G, confirming ring oscillator functionality.

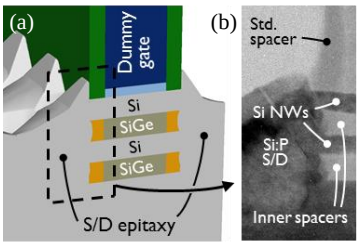

Fig. 7. (a) Schematic representation of a device structure after inner spacer formation (orange) and S/D epitaxy (Coventor® image). (b) TEM image after S/D epitaxy.

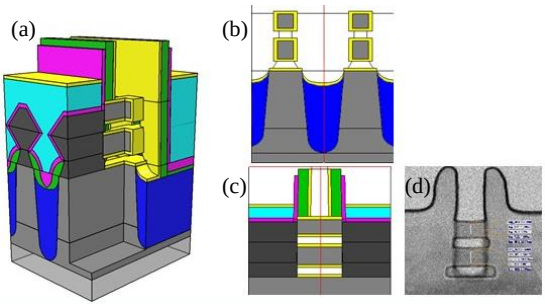

Fig. 8. GAA OCD model: (a) 3D representation, and (b) – (c) cross sections across and along Si nanowires. (d) TEM cross section along Si nanowires suspended in an RMG gate trench.

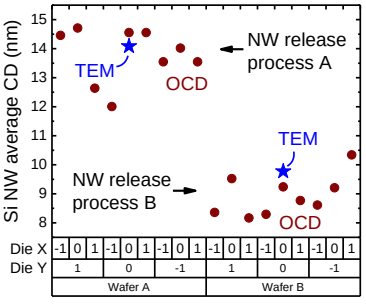

Fig. 9. Si NW CD differences for NW release processes A and B extracted from OCD (circles) and TEM (stars).

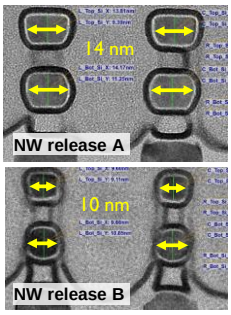

Fig. 10. Si nanowire TEMs for release processes A and B with different NW CD.

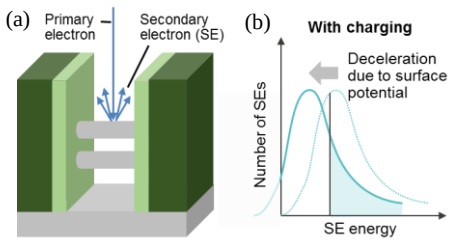

Fig. 11. (a) Primary and secondary electrons during top-down SEM. (b) Energy spectra of secondary electrons w/ and w/o NW charging. The vertical line indicates the threshold energy for voltage-contrast imaging.

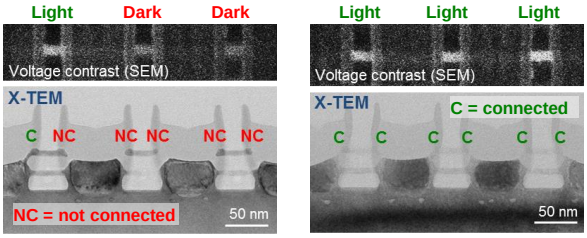

Fig. 12. Comparison between top-down SEM voltage-contrast images (top) and cross-sectional TEM images (bottom) of stacked Si NWs. Top NWs with interrupted S/D connections appear dark in top-down voltage-contrast SEM attributed to charging-induced spectral shift of the secondary electron distribution.