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Investigation of Full Bias Space Degradation in Nanosheet nFETs with HfO_2 Gate Dielectric by 3D-KMC Method

Wangyong Chen[1], Linlin Cai[1], Yun Li[1],Kunliang Wang[1], Xing Zhang[1, 2], Xiaoyan Liu[1] and Gang Du[1*]
[1] Institute of Microelectronics, Peking University, Beijing 100871, China.
[2] National Key Laboratory of Science and Technology on Micro/Nano Fabrication, Beijing 100871, China.
[*] Phone: +86 13810000259 Email: gangdu@pku.edu.cn , xyliu@ime.pku.edu.cn

Abstract

A 3D-Kinetic Monte Carlo (KMC) simulator is developed to evaluate degradation and variability with arbitrary Vg/Vd bias combinations. Excellent agreement in different degradation modes with experimental data are shown. Utilizing the simulator, threshold voltage degradation (ΔV_{th}) considering the impact of interface state and bulk trap in the Nanosheet nFETs with HfO_2 dielectric is investigated over the full bias space. The results show HCI exhibits more serious ΔV_{th} and suffers more variation due to the dominant contribution of interface state.

1. Introduction

Time-dependent reliability and variability, such as hot carrier injection (HCI), bias temperature instability (BTI), threaten significantly the operating lifetime of the device with aggressive scaled dimensions [1-2]. However, limited set of measured bias combinations or separate simulation of BTI and HCI are not sufficient for projecting the degradation to operation conditions. Moreover, interface trap and bulk trap contribution to the degradation and variability under different bias combinations are hard to distinguish from measurements. Thus physics-based trap behavior simulation is necessary for comprehending degradation with arbitrary Vg/Vd bias combinations. In this work, the developed 3D-KMC simulator considering multi-trap microscopic physical mechanisms is verified by experiment to capture degradation and variability over the full bias space, including all degradation modes in the unified system. With the simulator, the degradation induced by different traps under three degradation modes are compared and threshold voltage degradation (ΔV_{th}) mapping in Nanosheet nFETs with HfO_2 gate dielectric is also given.

2. Simulation Framework and Verification

The defect behaviors in gate dielectrics simulated by 3D-KMC are shown in Fig. 1, including the trapping, detrapping, generation, recombination and multiple traps coupling. The full-coupled multi-physical processes are driven by electrical field, carrier energy and temperature. The generation/recombination of interface state and bulk trap follow the truncated harmonic oscillator model [3-4] and chemical reaction model [5], respectively. Besides, the trapping and detrapping rate obeys nonradiative multi-phonon (NMP) model [6]. The integrated simulation flowchart is shown in Fig. 2. Detailed equations used in the 3D-KMC simulator are listed in Table. I. Fig. 3 demonstrates the simulation of PBTI effect in the nMOSFETs under different Vg biases, exhibiting excellent agreement with experiment [7]. And the simulation of HCI in nFinFETs under Vg/Vd 2.0V/2.0V bias also fits well with measurement [8], as shown in Fig. 4. Therefore, the simulator can achieve reliability evaluation of different degradation modes in the unified framework.

3. Results and Discussions

The degradation over the full bias space in the three-layer horizontally stacked Nanosheet nFETs structure with 0.4nm thickness SiO2 and 3.6nm thickness HfO2 gate dielectric is investigated by 3D-KMC method, see Fig. 5. A set of parameters are used for next simulation of HfO_2 based Nanosheet nFETs, listed in Table. II.

The time evolution of trap distributions in a layer Nanosheet including interface state and bulk trap under Vg/Vd 1.5V/1.5V stress is illustrated in Fig.6, showing the charged interface state are dominant compared to bulk traps. Fig. 7(a) and Fig. 7(b) show the statistical average interface trap number and bulk trap number of three typical degradation modes obtaining from 200 samples, respectively. The interface state is maximum in HCI mode while bulk trap contributes the most in degradation induced by BTI stress. Fig. 7(c) demonstrates threshold voltage shift in three different degradation modes. It can be seen that both the ΔV_{th} induced by HCI (Vg/Vd 1.5V/1.5V) and Off state stress (Vg/Vd 0V/1.5V) are severer than BTI modes (Vg/Vd 1.5V/0V) even though more bulk traps are induced by BTI stress. Because the interface state is dominating and captures carriers more easily. Cumulative distribution of ΔV_{th} after 100s BTI, HCI and Off state stress is plotted in Fig. 8(a) and the variation of ΔV_{th} is shown in Fig. 8(b), indicating maximal ΔV_{th} variation in HCI mode and minimal ΔV_{th} variation in BTI mode. The ΔV_{th} mapping of Nanosheet nFETs over the full bias space is presented in Fig.9. The maximum ΔV_{th} is 22mV after 100s stress.

4. Conclusion

3D-KMC simulator based on multi-trap behaviors is developed for investigating full bias space reliability and variability. The degradation mapping of Nanosheet nFETs is presented and the contribution of interface trap and bulk trap to total degradation under typical degradation modes are demonstrated, indicating that ΔV_{th} as well as variation induced by HCI are serious than BTI and Off state stress.

Acknowledgments

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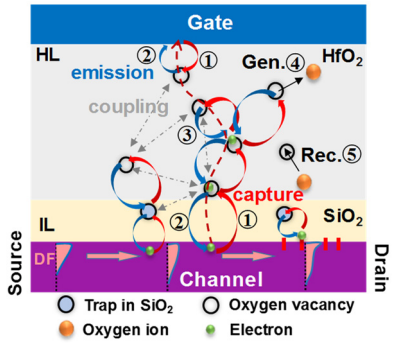

Fig.1 Defect activities including interface traps and bulk traps in gate dielectric are simulated by 3D-KMC.1).trapping from channel/gate, 2) detrapping to channel/gate, 3) tunneling between two traps, i.e. trap interaction, 4) trap generation, 5) trap recombination.

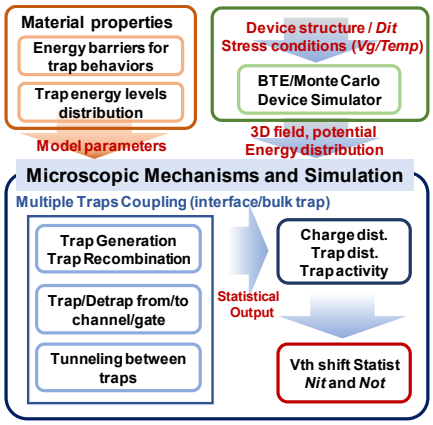

Fig.2 3D-KMC simulation flowchart for the evaluation of full bias space degradation induced by multiple traps.

Table. I Equations used for trap behaviour simulation in 3D-KMC simulator.

Trap: $k_c = \delta_{nc} v_n n \exp\left(-\frac{u_c - \lambda(F/F_0)^\rho}{k_B T}\right)$ (1)

Detrap: $k_e = \delta_{ne} v_n N_c \exp\left(-\frac{u_e + \lambda(F/F_0)^\rho}{k_B T}\right)$ (2)

Trap to trap: $k_{ij} = T_{ij} f_c \exp\left(-\frac{\varepsilon_{ij}}{k_B T}\right)$ (3)

Bulk trap generation/recombination:

$P_g = f_g \exp\left(-\frac{E_a - \gamma F}{k_B T}\right)$ (4) $P_r = f_r \exp\left(-\frac{E_r}{k_B T}\right)$ (5)

Interface state generation/recombination:

$P_{AB,n} = \int f(E)\, g(E) \sigma_0 (E - E_a + E_i)^p v(E) dE$ (6.1)

$P_{MVE} = \int f(E)\, g(E) \sigma_0 (E - \hbar\omega) v(E) dE$ (6.2)

$P_u = P_{MVE} + f_e \exp\left(-\frac{\hbar\omega}{k_B T}\right)$ (6.3) $P_d = P_{MVE} + f_e$ (6.4)

$P_{ig,n} = P_{AB,n} + f_e \exp\left(-\frac{(E_a - E_i)}{k_B T}\right)$ (6.5)

$P_{ig} = \frac{1}{k} \sum_n P_{ig,n} \left(\frac{P_u}{P_d}\right)^n, k = \sum_n \left(\frac{P_u}{P_d}\right)^n$ (6) $P_{tr} = f_e \exp\left(-\frac{E_{tr}}{k_B T}\right)$ (7)

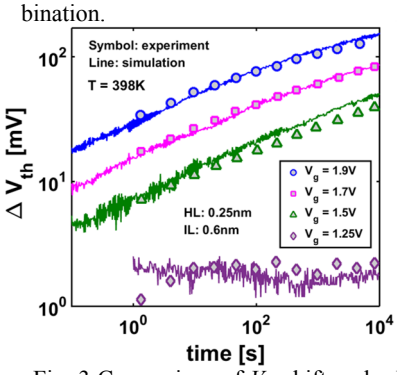

Fig. 3 Comparison of V_{th} shift under PBTI stress between 3D-KMC simulation and experiment [7].

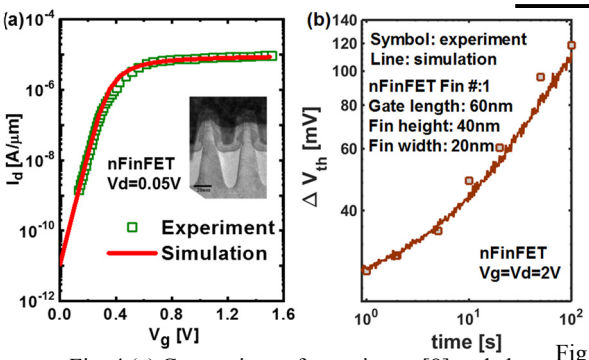

Fig. 4 (a) Comparison of experiment [8] and electrical performance simulated by TCAD (b) HCI simulated by 3D-KMC method compared to experiment under Vg/Vd 2V/2V bias.

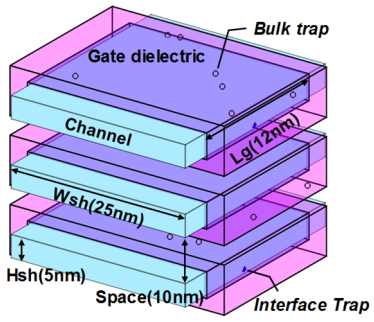

Fig. 5 Schematic of three-layer horizontally stacked Nanosheet structure used in this work, 0.4nm thickness interfacial layer (IL) and 3.6nm thickness high-k layer (HL) are applied to gate dielectric.

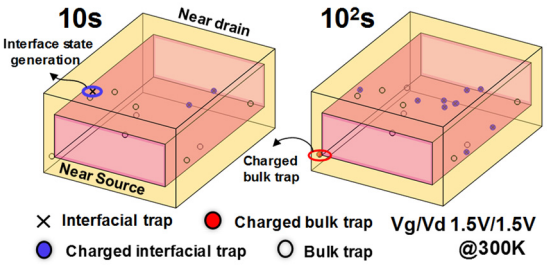

Fig. 6 The trap distributions including interface state and bulk trap in a layer Nanosheet under 10s and 100s Vg/Vd 1.5V/1.5Vstress, respectively. Time evolution of trap generation and charge are also shown.

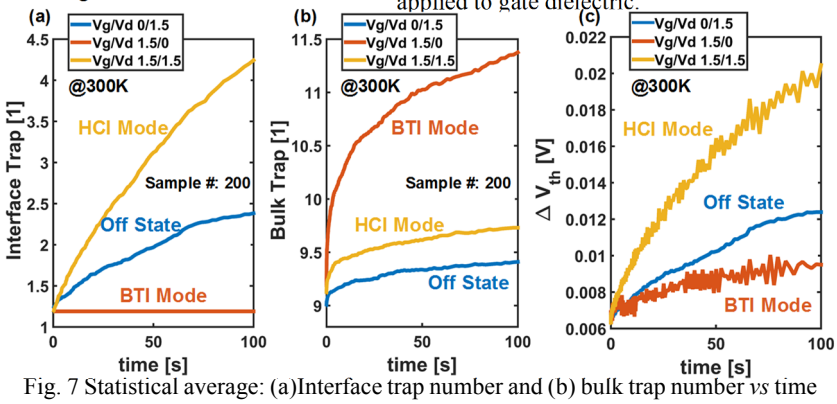

Fig. 7 Statistical average: (a)Interface trap number and (b) bulk trap number *vs* time under three different bias conditions, (c) V_{th} shift under three degradation modes.

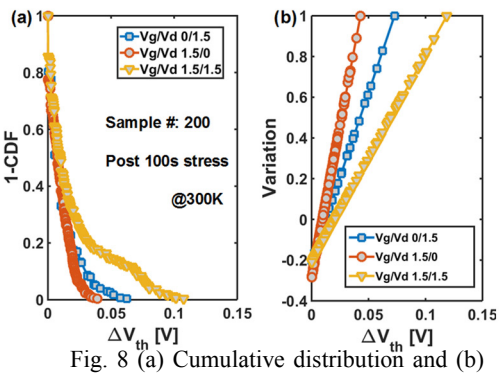

Fig. 8 (a) Cumulative distribution and (b) variation of ΔV_{th} after 100s stress under three degradation modes.

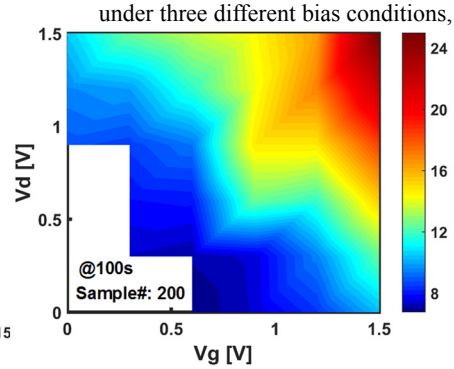

Fig. 9 Mapping of V_{th} degradation in Nanosheet nFETs over the full bias space after 100s stress.

Para.	HL	Para.	HL	IL
E_{a0}	2.55eV	u_{c0}	0.77eV	0.6eV
E_{r0}	1.1eV	u_{e0}	0.47eV	0.55eV
σ_{Ea}	0.36eV	σ_c	0.16eV	0.2eV
σ_{Er}	0.2eV	σ_e	0.1eV	0.1eV
γ	0.85nm	ρ	1.5	1
$u_{c,e}$	$N(u_{c0,e0}, \sigma_{c,e})$	λ	0.05eV	0.04eV
$E_{a,r}$	$N(E_{a0,r0}, \sigma_{Ea,Er})$	F_0	10^2V/cm	10^2V/cm

Region	HL(HfO_2)	IL(SiO_2)	Interface State
Trap density	~5×10^{18} cm^{-3}	~10^{18} cm^{-3}	~$10^{11}cm^{-2}$

Interface State: $\hbar\omega$=0.075eV p=11 E_a=1.5eV f_e=0.1ps^{-1}

Table. II Parameters used in 3D-KMC simulations, detailed physical meanings are shown in [9].