Extended Abstracts of the 2018 International Conference on Solid State Devices and Materials, Tokyo, 2018, pp159-160

Challenges and Opportunities for Vertical Nanowire FETs: Device Design and Fabrication

A. Veloso, P. Matagne, T. Huynh-Bao, G. Eneman, R. Loo, K. Wostyn, S. Brus, J. Boemmels, D. Mocuta, and J. Ryckaert
Imec, Kapeldreef 75, 3001 Leuven, Belgium
Tel.: +32-16-28 17 28, Email: Anabela.Veloso@imec.be

Abstract

We report on vertical nanowire (NW) FET devices (VNWFETs) with a gate-all-around (GAA) configuration, attractive for enabling denser circuits with increased layout efficiency such as ~20-30% denser SRAMs with improved read and write stability and up to 12× smaller MRAMs as compared to cells built with finFETs or lateral NWFETs as the SRAM cell transistors or memory selector. Focusing on the critical aspect of variability control, we present a thorough evaluation of the impact of gate misalignment (as well as NW size and doping, N_{NW}) on the DC and AC characteristics of inversion-mode (IM) *vs.* junctionless (JL) devices, and introduce a novel integration scheme to obtain VNWFETs immune to it. Here, self-aligned spacers are built relying on different oxidation kinetics for Si and SiGe. Lastly, we explore using vertical nanosheet (NS) *vs.* NW structures on various substrates, and investigate VFET geometry optimizations (e.g., gate length (L_{gate}), pillars height and doping) to boost the performance and reduce its intrinsic delay.

1. Introduction

As conventional CMOS scaling is reaching its physical limits and facing interconnect routing congestion [1,2], novel transistor architectures such as vertical GAA-NWFETs appear promising to overcome some of these limitations, while offering excellent electrostatics in 3D layout configurations. Their L_{gate} is defined vertically and can thus be relaxed without layout area penalty for optimized performance [3-5]. As for doping, the JL concept is an interesting option thanks to its process simplicity and reliability benefits due to lower E_{ox} at operation conditions [4-7]. However, due to random dopant fluctuations, acceptable time-zero, time-dependent variability, and mismatch (A_{VT}) values can only be obtained if N_{NW} is kept low enough ($N_{NW} \leq 1\times10^{19}$ at/cm^3), with highly doped source/drain (S/D) thus desirable for series resistance ($R_{S/D}$) reduction (hence higher I_{ON}) and improved contacting [4,5]. An additional source of variability and a key integration challenge for these devices lies therefore on the vertical alignment of the gate electrode with regard to the S/D as that is not a self-aligned process in contrast to finFETs or lateral NWFETs. This will be addressed in this work, together with the demonstration of a novel, simplified scheme to overcome such issues, while exploring further options for performance boost to enable higher value, highly scaled circuits with tight variability control, as exemplified in Figs. 1 and 2 [3,8].

2. Device fabrication

Schematics and an example of a TEM image from reference Si-based vertical GAA-NWFETs can be seen in Figs. 1 and 3, with the fabrication details provided in refs. [4,9]. In-situ doped Si epi is used for the pillars, while the gate is implemented with a gate-first or replacement-metal-gate scheme [9]. With the novel integration flow, three stacked layers of in-situ doped epi (SiGe/Si/SiGe) are key to form the wires, followed by self-aligned spacers (Fig. 6).

3. Results and discussion

Fig. 3 shows the V_T control obtained for simplified VNWFETs built using uniformly doped wires ($N_{NW}\sim2\times10^{18}$ at/cm^3) and a doped substrate as bottom electrode (TEM in Fig. 3a). The tight V_T and ΔV_T distributions (Fig. 3b) attained despite a NW diameter (d_{NW}) range of $\Delta d_{NW}\sim13$nm (Fig. 3c) indicate a wide d_{NW}-V_T process window for small wires with sufficiently low N_{NW}, a requirement for controlled JL variability. Introduction of highly doped S/D regions to boost I_{ON} (via highly doped layers in the epi stack grown to form the NWs) brings an additional source of variability specific to these FETs since their gate and S/D are not self-aligned, as confirmed by the TCAD results in Figs. 4 and 5. Indeed, Fig. 4 shows that gate misalignment leads to considerable I_{ON} degradation, with gate underlap creating a larger series resistance and a stronger impact on the source side (e.g., I_{ON} reduced by 64%/37% for JL devices with $N_{NW}\sim2\times10^{18}$ at/cm^3 and 10nm underlap towards S/D, respectively). The impact is worst for IM *vs.* JL VFETs and is less pronounced with increased N_{NW}, though the latter comes at the expense of increased variability and DC performance loss. A negative (positive) misalignment shifts the top of the potential barrier towards the source (drain) and so, for small misalignments, a shifting towards the drain opposes the barrier lowering and can explain some asymmetry in DIBL, I_{OFF}. As the effective L_{gate} is reduced with gate underlap, that degrades I_{OFF} and the short channel electrostatics (i.e., SS, DIBL). Fig. 4 indicates these to be acceptable for a wider underlap/overlap range. Fig. 5 shows limited fluctuations in the total gate capacitance (C_{GG}) due to gate misalignment, with a small impact on switching speed.

To obtain vertical devices immune to gate misalignment, a novel integration scheme is proposed in Fig. 6 wherein the Si channel is vertically surrounded by SiGe regions. Selective oxidation of SiGe *vs.* Si (with a low temperature steam anneal) leads to the formation of SiGe-oxide spacers, self-aligned to the Si channel, as illustrated by the TEM images in Fig. 6. Here, similar spacer widths are obtained for wires of varying d_{NW} with identical SiGe thicknesses. SIMS profiles of $Si_{0.75}Ge_{0.25}$/Si/$Si_{0.75}Ge_{0.25}$ epi stacks grown for building such devices are shown in Fig. 7, wherein various boron (B) doping concentrations in the Si region were implemented to target p-type JL VNWFETs of varying N_{NW}. Both SiGe layers are highly B doped, with sharp profiles measured for the stacks as-grown and after undergoing an anneal done to mimic later thermal budget steps in the flow. 25% Ge is targeted, with the reliability of the resulting SiGe-oxide (e.g., its breakdown voltage) in line with that from other typical spacer materials. Also, no (or negligible) impact of p or n-type doping in the $Si_{0.75}Ge_{0.25}$ oxidation kinetics is seen in Fig. 8. The TCAD results in Figs. 9-11 show that, besides exhibiting immunity to gate misalignment, these Si/SiGe devices can match or even exceed the performance of reference Si VFETs, for both DC and AC, upon tuning of the spacers thickness/width and the doping in the regions underneath them. For the spacers configuration in Figs. 9 and 10, an ungated Si area is created under the spacers which increases $R_{S/D}$ (less so with increased doping in that region), being smaller for thinner spacers which are thus beneficial for I_{ON}. However, as shown in Fig. 10, thinner spacers also lead to larger parasitic capacitances. The optimum spacers thickness is therefore derived from a trade-off between the devices AC and DC performances, with 5nm spacers appearing to be a good compromise in this case. The results in Fig. 9 also highlight that in the case wider S/D areas *vs.* d_{NW} are implemented, they are beneficial for I_{ON} due to lower $R_{S/D}$. Similar results can be obtained for other spacer configurations, namely the one represented in Fig. 11 wherein n-type VNWFETs with 10nm diameter pillars are investigated. Here, identical I_{ON} is computed for Si-only devices or with the Si channel vertically neighbored by SiGe areas (covered by spacers), provided doping and the spacers width are optimized. The optimal spacers (e.g., their thickness) will be set also by AC.

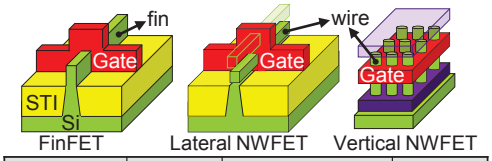
Similarly to lateral NW or NS FETs [10,11], Fig. 12 shows that significantly higher current drivability, for both NMOS and PMOS, can be expected for VFETs made of VNSs with higher effective width *vs*. VNWs with a circular cross-section, while a different substrate orientation can also help boost n or p-type devices. In the absence of strain (for further increasing I_{ON}), this can be an interesting option, especially if only n or p-type devices are required as is the case for the MRAM selector transistor discussed in Fig. 1. Fig. 13 illustrates a possible implementation of it, also showing the impact of some device geometry features on I_{ON}, C_{GG} and its intrinsic delay (CV/I), while maintaining SS and DIBL.

4. Conclusions

A novel integration scheme with Si/SiGe pillars and self-aligned spacers is demonstrated to yield JL or IM VNWFETs immune to gate misalignment for DC/AC, enabling scaled circuits with tight variability control. The use of VNS *vs.* VNW on various substrates and device geometries was also explored to boost performance.

References

[1] K. J. Kuhn, IEEE Trans. Elect. Dev., 59(7) (2012) 1813; [2] A. V.-Y. Thean *et al.*, VLSI Tech. Dig. (2015) 26; [3] T. Huynh-Bao *et al.*, SPIE Proc. 9781 (2016) 978102; [4] A. Veloso *et al.*, VLSI Tech. Dig. (2016) 138; [5] A. Veloso *et al.*, SSDM Tech. Dig. (2017) 221; [6] J.-P. Colinge *et al.*, Nature Nano. (2010) 225; [7] A. Veloso *et al.*, VLSI Tech. Dig. (2015) 138; [8] R. Appeltans *et al.*, SPIE Proc. 10148 (2017) 101480G; [9] A. Veloso *et al.*, ECS Trans. 80(2) (2017) 3; [10] H. Mertens *et al.*, IEDM Tech. Dig. (2017) 828; [11] N. Loubet *et al.*, VLSI Tech. Dig. (2017) 230; [12] M. H. Na *et al.*, IEDM Tech. Dig. (2002) 121.



FinFET SRAM	VNWFET SRAM	FinFET + MRAM		VNWFET + MRAM
High-density cell (111)	1 VNW per VFET	regular BEOL	optimized BEOL	1 VNW per VFET
Baseline cell size (Ref)	0.75×	1/3×	1/4×	1/12×
6MP x 2CPP	4.5MP x 2CPP	2MP x 2CPP	2MP x 1.5CPP	1MP x 1CPP

Fig.1 – Schematics of triple-gate finFETs and GAA-NWFETs which can be built in a lateral or vertical configuration. A benchmark comparison of memory cell sizes, defined by the metal pitch (MP) × contacted poly (gate) pitch (CPP), using these various devices as the SRAM cell transistors or as the selector in the case of MRAM is shown on the table [3,8].

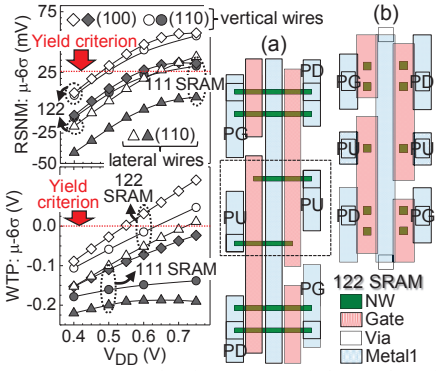


Fig.2 – 6σ margin (i.e., μ-6σ) of the read static noise margin (RSNM, on top) and write-trip-point (WTP, at the bottom) for SRAM cells with similar area, using lateral (a) or vertical (b) GAA-NWFETs with L_{gate}=14/30nm and d_{NW}=7/10nm, respectively, and the design rules in ref.[3]. VNWFETs yield better performing SRAMs, allowing a smaller V_{DD}.

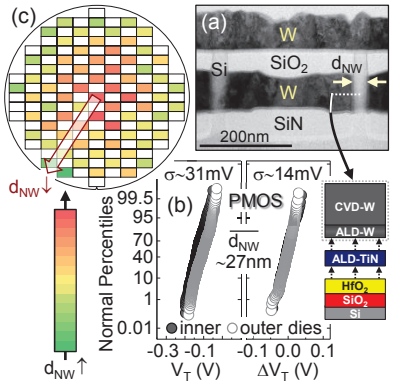


Fig.3 – JL Si-based VNWFETs with low enough channel doping (here, N_{NW}~2×10^{18} at/cm^3) allow a considerably wide process window for the NW size, V_T and V_T-mismatch control (data for Δd_{NW}~13nm at V_{DS}=-1V, with the d_{NW} distribution similar to that shown by the wafer map in c)).

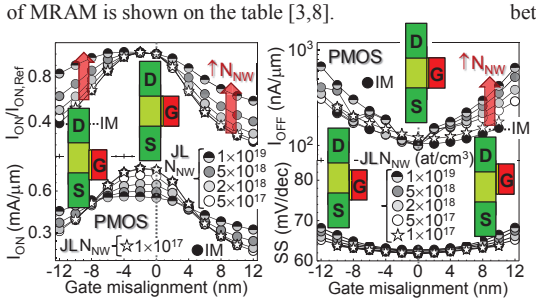


Fig.4 – TCAD simulations show that I_{ON} is sensitive to gate misalignment in vertical GAA-NWFETs. The impact is stronger for IM devices, decreasing for higher N_{NW} JL FETs. The corresponding I_{OFF} and SS increases are seen to be acceptable within a certain underlap/overlap range (data calculated for VNWFETs with d_{NW}=10nm, L_{gate}=30nm, and $N_{S/D}$=1×10^{20}at/cm^3).

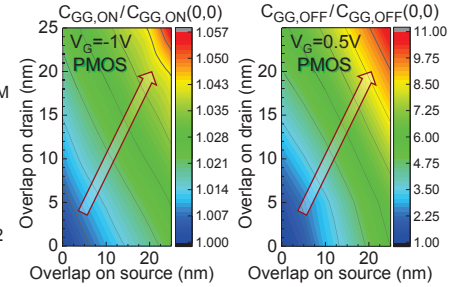


Fig.5 – Limited impact from gate misalignment on C_{GG} in the on-state (left plot) and off-state (right plot) can be obtained within a certain overlap range (TCAD data for d_{NW}=7nm, L_{gate}=60nm, N_{NW}=1×10^{19}at/cm^3, $N_{S/D}$=1×10^{20}at/cm^3).

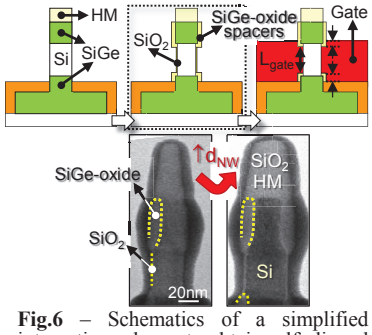


Fig.6 – Schematics of a simplified integration scheme to obtain self-aligned (SiGe-oxide) spacers for VFETs, as highlighted by the TEM images. It relies on the oxidation kinetics of Si and SiGe.

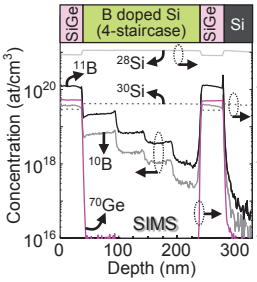


Fig.7 – SIMS profiles of SiGe/Si/SiGe stacked epi layers grown in-situ for p-type JL VNWFETs: the SiGe layers are highly B doped, and 4 different B doping concentrations are defined in the middle Si region to target various N_{NW} devices.

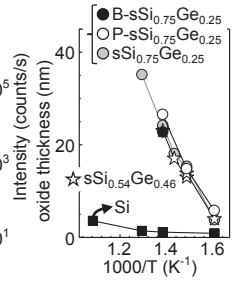


Fig.8 – Si and SiGe exhibit different oxidation kinetics, with a negligible impact of boron (B) or phosphorus (P) doping seen for $Si_{0.75}Ge_{0.25}$.

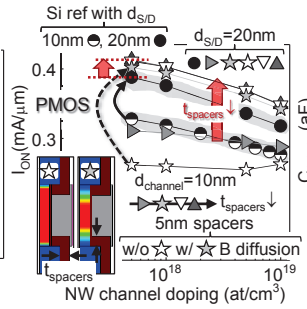


Fig.9 – TCAD simulations show that the Si/SiGe devices from Fig.6 can match or even exceed the DC performance of Si VNWFETs for optimized spacers thickness and doping in the regions underneath the spacers.

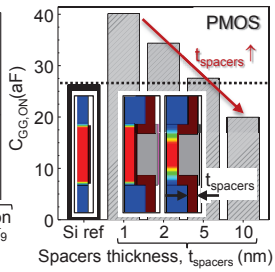


Fig.10 – Si/SiGe VFETs with thicker spacers have smaller parasitic capacitance values. Overall, a trade-off between the devices AC and DC (in Fig.9) performances yields the optimal spacers.

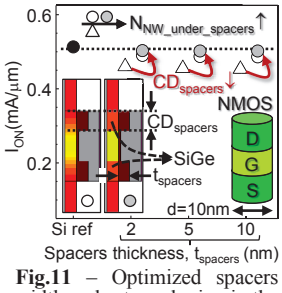


Fig.11 – Optimized spacers width and n-type doping in the SiGe areas (under the spacers, neighboring the Si channel with d_{Si}=d_{SiGe}) are key knobs for high performing n-VFETs, matching the Si reference, and immune to gate misalignment.

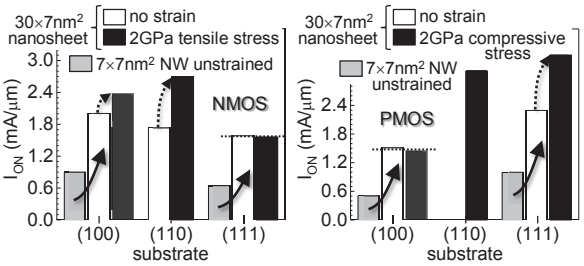


Fig.12 – Ballistic current simulations yield higher drive currents (I_{ON}), as normalized by wire pitch, for vertical NSs (30×7nm^2) with (110) for their wider sidewalls *vs.* vertical NWs (7×7nm^2), for both PMOS and NMOS built on (100), (110), and (111) Si substrates. The current flow direction is the same as the substrate orientation in all cases, with performance further boosted via stress (I_{ON} calculated at V_G=$V_{G,OFF}$±0.6V for I_{OFF}=100nA/μm, and 35nm NW/NS pitch).

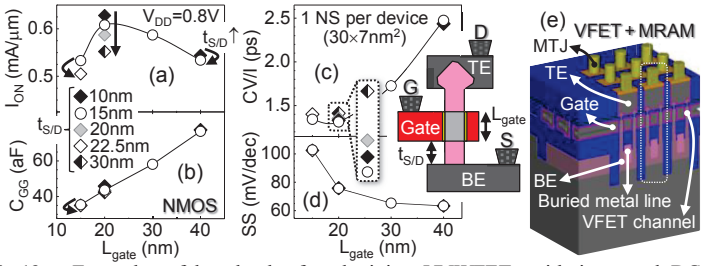


Fig.13 – Examples of key knobs for obtaining VNWFETs with improved DC performance and reduced intrinsic device delay (CV/I) are illustrated by the TCAD results in a-d). Here, the data were calculated for n-type devices consisting of one 30×7nm^2 VNS with (110) for its wider sidewalls on a (100) substrate, at V_{DD}=0.8V and I_{OFF}=100nA/μm. Their effective drive currents (I_{eff}, as defined in ref.[12]) were used to predict CV/I. As mentioned in Fig.1, such transistors can be adopted as the selector for ultimate scaled MRAM cells, with its dimensions (and also the number of VNW or VNS per device – 2 in e)) adjusted to meet performance requirements.