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A CMOS-Compatible Current Boosting Scheme in 14 nm FinFET Technology

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Abstract

A novel drive current boosting scheme is experimentally demonstrated in 14 nm baseline foundry process FinFET technology. A constant bias applied to the booster terminal results in a positive base current that is generated only at high gate voltage. The base current subsequently amplifies lateral bipolar current, boosting the current drive. The current boosting scheme results in ~2x drive current compared to standard FinFET. The amplification is off at low gate and/or low source/drain voltage, maintaining low off-state current. Scalability to 7 nm technology node is also shown using TCAD simulation.

1. Introduction

Steep sub-threshold slope transistors, such as impact ionization MOS, tunneling FET, and negative capacitance FET have been investigated to enhance transistor performance. Body bias engineering, such as dynamic threshold voltage MOSFET (DTMOS) has also been previously proposed to enhance drive current while maintaining off-state current. However, each of these approaches has its own drawbacks such as limited reliability, non-foundry compatible process, and limited Vdd range. Previously, we demonstrated a boosted MOS (βMOS) employing intrinsic vertical BJT as gate voltage controlled base current source (VCCS) by adding buried n-well formation process in 28 nm planar technology [1]. The concept of charge injection using gated npnp thyristor in SOI has also been reported [2]. In this paper, we experimentally demonstrate βMOS (**Fig. 1**) in baseline 14 nm bulk FinFET technology.

2. Results and Discussion

A SEM image of the fabricated βMOS with Lg=14 nm is shown (**Fig. 2**). Adjacent n-well regions are used to apply bias Vb to the booster region. **Fig. 3** shows a typical Id-Vg curve for two different booster terminal voltages Vb (Vb=0V and Vb=Vboost). Both conditions result in similar curves at low gate voltage (Vg) region. However, when a constant positive bias Vboost is applied to Vb, an on-state current (Ion) gain is observed at high Vg while maintaining the off-current (Ioff). As shown in Fig. 3, βMOS shows a higher drain current at lower Vd=0.7V compared to standard MOS (sMOS) at higher Vd=0.8V. The current boosting mechanism is described in **Fig. 4**. At high Vg and Vd, electrons from the source (emitter) creates impact ionization at the floating fin (base)-booster region (collector) junction and the generated holes flow into the fin (base) region. This base current then amplifies the lateral bipolar current, boosting Id [3]. **Fig. 5** shows the boosting at various Vdd. The current boosting ratio increases as Vdd decreases, implying that the boosting mechanism is more effective at lower Vdd and can result in lower operating power. A current gain of 84% is obtained at Vdd=0.6V. Further current boosting can be attained by increasing Vb, as increasing Vb will increase the drive current due to greater impact ionization. Further current boosting can also be achieved through process optimization of the booster region formation.

While higher Vb enhances the drive current boost, it is worthwhile to note that there is a limit to the boosting voltage. When Vb is greater than an upper limit for boosting, referred as Vmem>Vboost,max, the impact ionization process can be sustained even at Vg=Vd=Vs=0V. The self-sustaining impact ionization phenomenon can be utilized as static, bi-stable memory cell, referred to as Bi-SRAM (**Fig. 6**) [4].

TCAD results shows the impact ionization is active only at high Vg (**Fig. 7**). The energy band diagrams along the gate length direction shows that the source-to-channel potential barrier is lower when the Vboost is applied to the booster terminal. In order to study the scalability of the boosted transistor, 3D TCAD and mixed-mode simulation were conducted based on a 7 nm FinFET technology. **Fig. 8a** shows that the bipolar current contribution becomes distinctive at the on-state of the boosted mode. The mixed mode simulation of ring oscillator implemented with 7 nm FinFET 2-input NAND logic cells shows simultaneous 1.9x speed gain and 2.1x power reduction over sMOS as shown in **Fig. 8b**.

3. Conclusions

A boosted current FinFET is demonstrated on 14 nm baseline FinFET technology. A constant bias applied to the boost terminal results in ~2x drive current boosting at lower Vdd while maintaining the off-current. Furthermore, the same device structure and mechanism can also be utilized as bi-stable, CMOS-compatible, 1-transistor memory cell.

References

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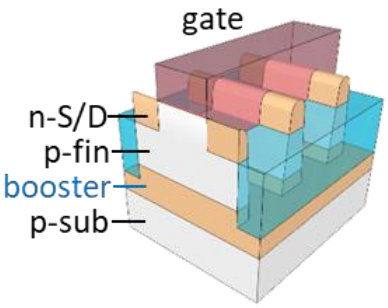

Fig. 1 Schematic illustration of proposed boosted FinFET.

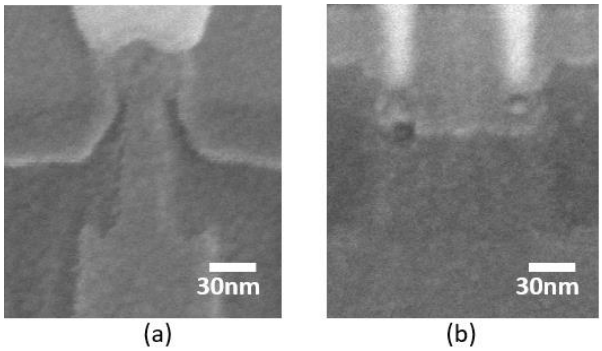

Fig. 2 SEM image of fabricated boosted FinFET cut-along (a) fin width and (b) gate length direction.

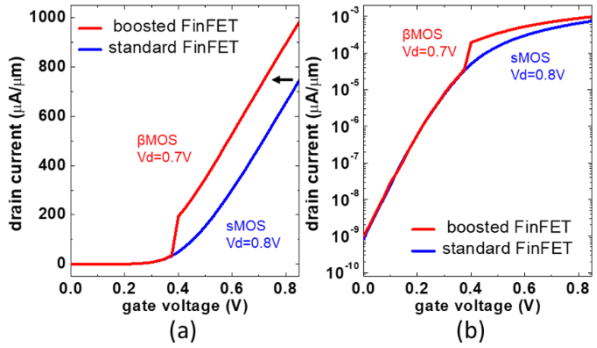

Fig. 3 Id-Vg characteristics of standard (Vb=0V) and boosted (Vb=Vboost) FinFETs in (a) linear and (b) semi-log scale.

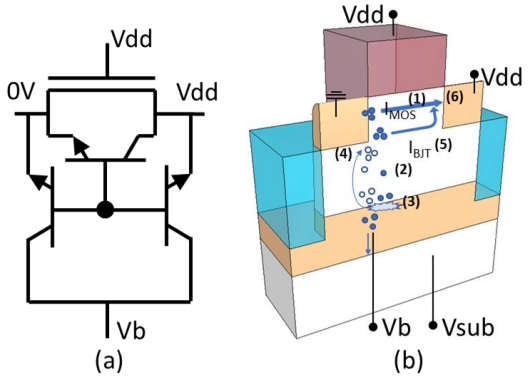

Fig. 4 (a) Equivalent circuit model and (b) drain current amplification mechanism in boosted FinFET

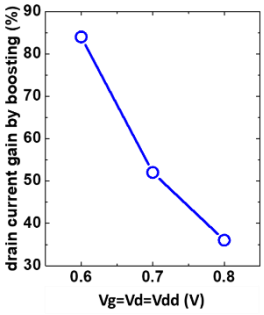

Fig. 5 Drain current gain through boosting mechanism for various Vdd.

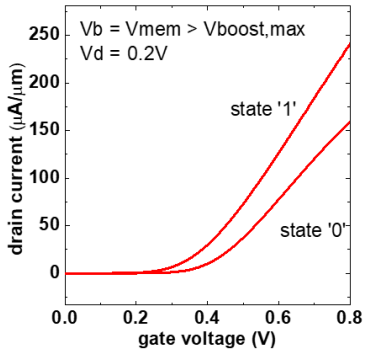

Fig. 6 Measured Id-Vg characteristic showing static memory behavior at Vb=Vmem>Vboost,max.

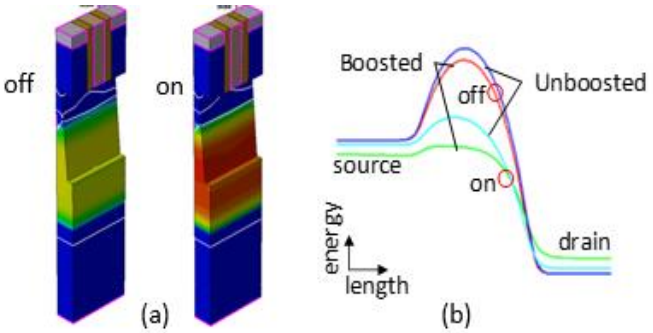

Fig. 7 (a) Simulation results of impact-ionization near depletion region and (b) energy band diagram of on- and off-states.

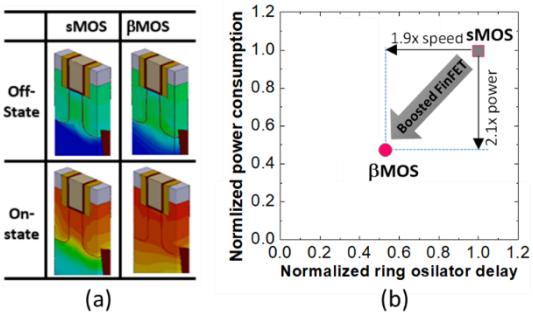

Fig. 8 Scalability study to 7 nm FinFET technology by simulation. (a) Current density map and (b) TCAD/RC/HSPICE result of power and delay of ring oscillator built on 2-input NAND logic cells.