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Temperature Effect on DIBL Variability in Bulk and SOTB MOSFETs

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Abstract

This paper presents a statistical study of temperature effect on drain-induced barrier lowering (DIBL) for the first time. We report a new finding that DIBL variability is reduced at high temperature due to the negative correlation between DIBL and its temperature coefficient dDIBL/dT. Physical mechanism of this phenomenon is discussed, and verified by 3D TCAD simulation.

1. Introduction

With deeper electronics penetration in everyday life such as IoT devices and health/medical devices, wide-range temperature applications are increasingly needed, therefore understanding temperature effect on device performance is of great importance. It is well known that high temperature alters or degrades device performance by reducing threshold voltage (V_t) and on-state drain current (I_{on}), as well as increasing subthreshold slope (SS) and off-state current (I_{off}). Drain-induced barrier lowing (DIBL) is a crucial indicator of short channel effects, and it is reported to have temperature dependence [1-3].

Meanwhile, statistical variability is one of the critical problems in scaled MOSFETs, which is also influenced by temperature. The variability of V_t (linear) and I_{on} at high temperature have been well studied [4-5]. On the other hand, DIBL variability has significant impact on SRAM and analog circuits [6-8]. The variability of DIBL due to source-drain positional asymmetry has been comprehensively studied [7-9]. To the best of our knowledge, however, temperature effect on DIBL variability has not been studied yet.

In this work, temperature effect on DIBL was statistically studied for the first time. Experimental results show that the mean value of DIBL increases, but DIBL variability decreases as temperature rises, due to the negative correlation between DIBL and its temperature coefficient dDIBL/dT. Physical mechanism of this new finding was explained, and verified by 3D TCAD simulation.

2. Experimental Methods

1k (=1024) bulk and silicon-on-thin-box (SOTB) nFETs (L/W=60nm/120nm) fabricated by a 65nm technology [10] were measured at room temperature (RT=25°C) and high temperature (HT=100°C) using a device matrix array (DMA) test element group (TEG) [11]. Drain bias was set at 50mV and 1.2V for linear and saturation region. Threshold voltage (V_t) was calculated using constant current method at reference current $I_0=W/L\times10^{-7}$A. DIBL was defined as $(V_{tlin}-V_{tsat})/(V_{dsat}-V_{dlin})$. Temperature coefficient of V_t ($|dV_t/dT|$) was defined as $(V_{tRT}-V_{tHT})/(HT-RT)$, note that absolute value is used here to describe how much V_t decreases at HT. Temperature coefficient of DIBL (dDIBL/dT) was defined as $(DIBL_{HT}-DIBL_{RT})/(HT-RT)$.

3. Results and Discussion

Fig.1 shows the correlations between V_{tRT} and V_{tHT}, in both linear and saturation region. Very strong correlations ($\rho\approx1$) indicate that there is no anomalous change between RT and HT. Fig.2 shows the Q-Q plots of $DIBL_{RT}$ and $DIBL_{HT}$. It is found that <DIBL> increases, but σDIBL decreases as temperature rises. DIBL variability reduces at HT owing to the negative correlation between $DIBL_{RT}$ and dDIBL/dT, as shown in Fig.3. The negative correlation indicates that transistors with small $DIBL_{RT}$ are likely to degrade more at HT, and this correlation exists in both bulk (ρ=-0.61) and SOTB (ρ=-0.50) FETs. Bulk FETs have larger DIBL and dDIBL/dT variability than SOTB due to random dopant fluctuation (RDF). Also, about 3% of bulk nFETs with larger $DIBL_{RT}$ show negative dDIBL/dT, but this phenomenon is not observed in SOTB nFETs.

For understanding the origin of negative correlation between DIBL and dDIBL/dT, 1k long channel (L/W=500nm/120nm) bulk nFETs were measured. Fig.4 shows scatter matrix of related parameters in short and long channel bulk nFETs. In long channel devices, DIBL is much smaller, but the negative correlation between DIBL and dDIBL/dT becomes stronger (ρ=-0.84), which serve as informative extreme cases. Notice peculiar triangular shapes for DIBL and dDIBL/dT related correlations (subplots L7~14).

To understand this, three extreme case transistors, i.e. (A) symmetrical potential, (B) higher source potential and (C) higher drain potential, were simulated, and the results were mapped on the scatter plots (Fig.5). It can be confirmed that these three cases correspond to the corners of the triangles [7]. Device C shows the largest DIBL, since its potential peak is influenced more by high drain bias (Fig.6). Referring to Sim2 and 5, there are strong positive correlations between V_t and its temperature coefficient $|dV_t/dT|$. Since devices B and C have similar V_{tlinRT}, but very different V_{tsatRT}, likewise for $|dV_{tlin}/dT|$ and $|dV_{tsat}/dT|$ (see Sim2 and 5). As a result, $dDIBL/dT= dV_{tlin}/dT–dV_{tsat}/dT=|dV_{tsat}/dT|–|dV_{tlin}/dT|$ deviates between devices B and C, in spite of the similar V_{tlinRT} (Sim11), device B showing larger dDIBL/dT than C. As for DIBL, the relationship is reversed; device C shows larger DIBL than B (Sim7). This finally leads to negative correlation between DIBL and dDIBL/dT (Sim15). As channel length reduces to 60nm, the difference between symmetrical and asymmetrical devices is not as obvious as that in long channel. Triangular correlations are weakened in subplots S7~14 because more devices locate in the “middle-state”, but their joint effects on the negative correlation between DIBL and dDIBL/dT should still exist.

To confirm this idea, reverse measurements by interchanging source/drain contacts were performed. In Fig.7, transistors with large DIBL_forward and small DIBL_reverse, which are considered to be similar to device C, show exceptionally small dDIBL/dT_forward, in agreement with the above considerations. Fig.8 shows the V_t behaviors of two measured transistors, which are believed to be similar to devices B and C. It can be confirmed that the higher source potential (smaller DIBL) device shows larger $|dV_{tsat}/dT|$, resulting in larger dDIBL/dT.

Finally, 3D Monte Carlo TCAD simulations were carried out in bulk nFETs with L/W=60nm/120nm. The asymmetry of source/drain originates from randomized grain (with two different workfunction values) in the gate. 100 bulk nFETs with smaller WF difference (0.1eV), while other 100 bulk nFETs with larger WF difference (0.2eV) were simulated. Fig.9 shows the simulated negative correlation between $DIBL_{RT}$ and dDIBL/dT. Also, negative dDIBL/dT is observed in some large variation cases, which is in good agreement with experimental results that negative dDIBL/dT only exists in bulk FET whose potential asymmetry is larger due to RDF.

4. Conclusion

It was experimentally found that DIBL variability is reduced at high temperature, due to the negative correlation between DIBL and dDIBL/dT. This negative correlation was explained and verified by 3D TCAD simulation.

References

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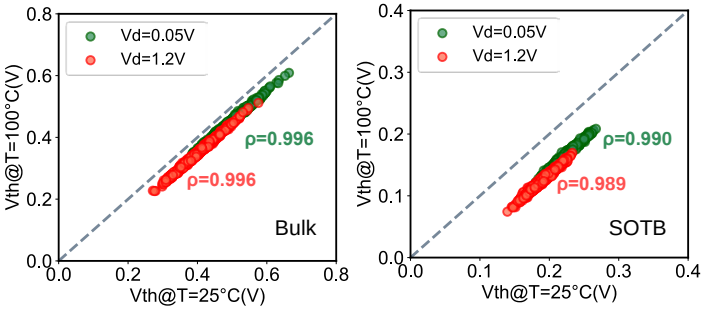

Fig.1. Correlation plots of V_{tRT} and V_{tHT}. (Left) bulk (Right) SOTB nFETs.

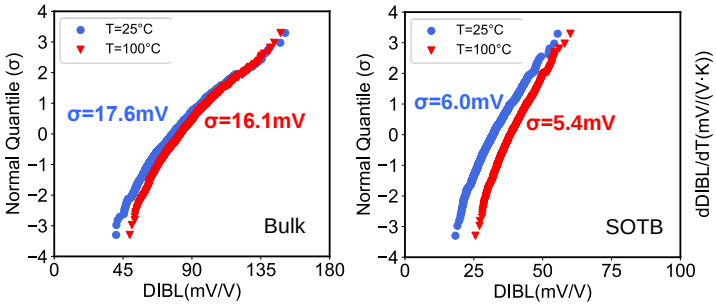

Fig.2. Q-Q plots of $DIBL_{RT}$ and $DIBL_{HT}$. (Left) bulk (Right) SOTB nFETs.

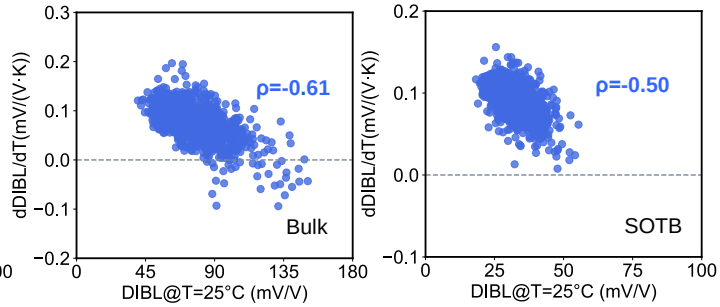

Fig.3. Negative correlations between $DIBL_{RT}$ and dDIBL/dT. (Left) bulk (Right) SOTB nFETs.

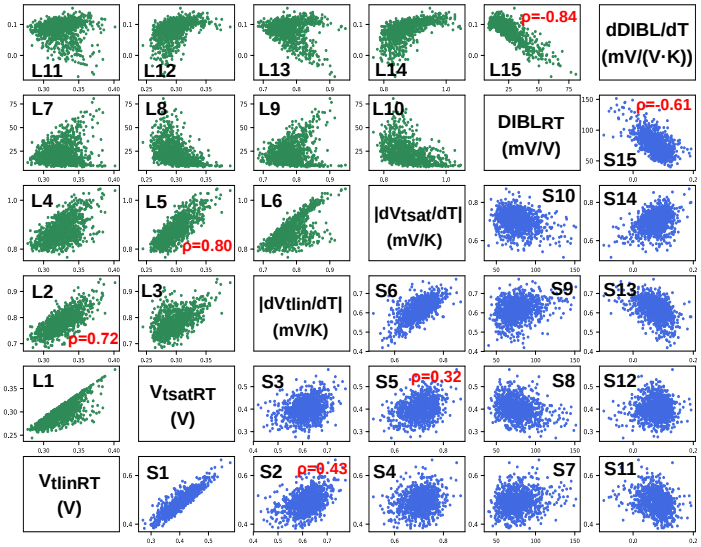

Fig.4. (Measurement) Scatter matrix of V_{tlinRT}, V_{tsatRT}, $DIBL_{RT}$ and their temperature coefficients. Green plots: 1k bulk nFETs with L=500nm (long channel). Blue plots: 1k bulk nFETs with L=60nm (short channel).

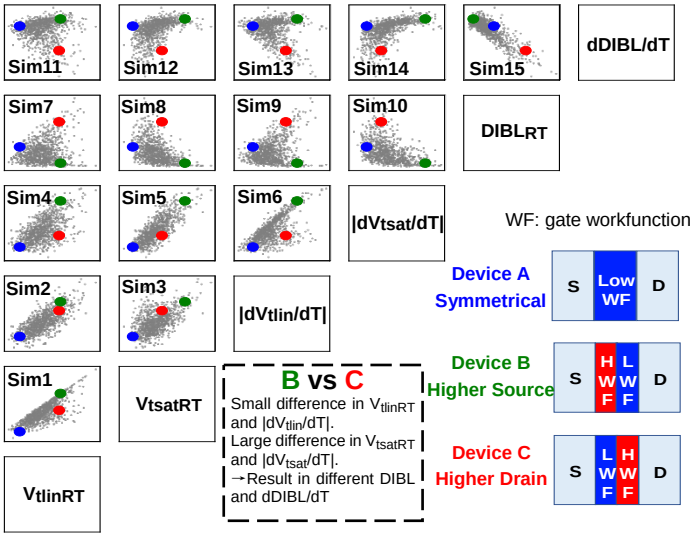

Fig.5. (Simulation) Scatter matrix of three typical devices. Blue: Device (A) with symmetrical potential distribution. Green: Device (B) with higher source potential. Red: Device (C) with higher drain potential. (Grey plots are measured long channel devices in Fig.4 as reference shapes)

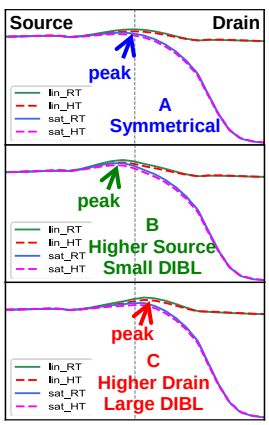

Fig.6. Potential profiles of A, B and C at a fixed Vg=0.4V (near V_{tlinRT} of A).

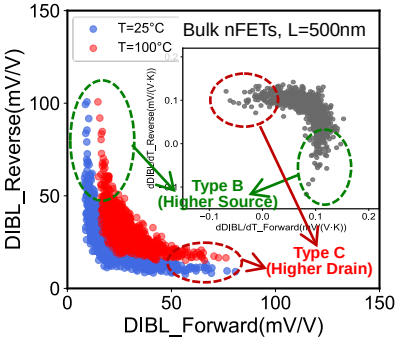

Fig.7. Comparison of forward and reverse measured $DIBL_{RT}$, $DIBL_{HT}$ and (inset) dDIBL/dT in bulk nFETs (L=500nm). Higher source potential devices turn to higher drain potential devices after changing S/D, and vice versa.

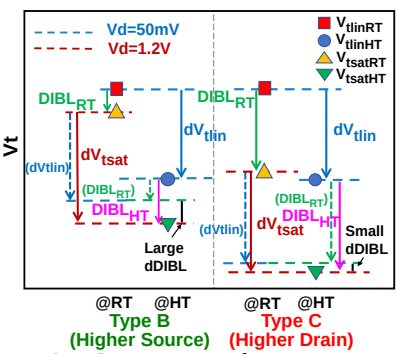

Fig.8. Comparison of two measured transistors representative for higher source /drain potential devices, with almost same V_{tlin} and $|dV_{tlin}/dT|$. Arrows stand for the decreased V_t by high temperature or DIBL. Dotted arrows are shifted copies for the calculation of dDIBL.

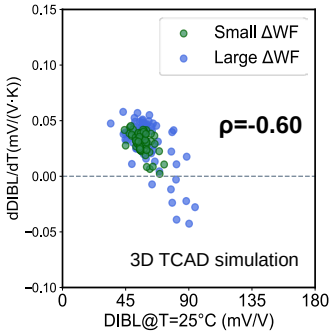

Fig.9. Simulated negative correlations between $DIBL_{RT}$ and dDIBL/dT in 200 random bulk nFETs by 3D TCAD. (Green) small WF difference (0.1eV). (Blue) large WF difference(0.2eV).