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Optimization of RTN FDSOI Device Performance for Analog/Mixed Signal and Low Noise Applications

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***Abstract*—Device noise performance is determined by circuit bias conditions. Trade-off between power efficiency and RTN (Random Telegraph Noise) must be identified. Integrations elements such as well–type and optimized interface quality are employed to improve device RTN. Front gate connected to back gate allows superior performance without additional integration complexity.**

1. Introduction

In state of the art analog circuits area consumption and optimum performance are limited by noise [1-2]. It has several origins: thermal noise, which is directly proportional to circuit temperature [3], Random Telegraph Noise (RTN) attributed to single trapping/de-trapping event of defects (D_{it}) located at the gate oxide-silicon channel interface [4] and translates in 1/f for uniform D_{it} distributions in the Si band gap [5]; and other types of noise which appear at high frequency regime [6]. In this paper, we focus on RTN and its correlation with the device integration, which is critical for analog applications operating at low frequency. Severe fluctuations of device drain current I_D due to RTN events can compromise the circuit functionality and thus limit its performance. Ad-hoc devices derived from 22nm FDSOI technology were used [7]. Next section discusses the correlation between circuit operating conditions and measured RTN. In section III and IV we show how the device integration and layout optimization can be tuned accordingly to circuit specifications to improve noise performance.

2. Impact of Operating Point on Device Noise

A typical CMOS differential amplifier (Fig. 1) illustrates the impetus for analog improvements to the process. The drain current standard deviation (σI_{Dn}) induced by oxide defects of the n-MOS input pair added to the p-MOS load σI_{Dp} sets the input-referred noise floor. High device transconductance g_m, however, attenuates the RTN impact. Hence, single device performances ($\sigma I_{Dn,p}$ and g_m) must be co-optimized to reduce the noise floor of the circuit. σI_D and transconductance are determined by circuit set point. The device operates in different regimes according to the chosen drain current I_D with consequent modulation of power efficiency (Fig. 2). The relative contribution of RTN events to I_D is a function of the used bias conditions as well (Fig. 3). Lower impact of σI_D is measured with high drain current. For optimum circuit optimization a trade-off between power efficiency and RTN contribution must be found during circuit design.

3. Optimization of Device Integration

The schematic of used device architecture is given in Fig. 4a. Silicon-on-Insulator (SOI) substrate wafers with a buried-oxide (BOX) thickness of ~ 20nm have been used. The silicon channel, featuring a final thickness of ~ 6nm was kept un-doped. The gate oxide of the fabricated devices includes a thick EOT of ~ 6.7nm suitable for analog applications and allowing a balanced top gate vs. back gate capacitance ratio of ~ 1/3. FDSOI technology offers the possibility to select among different integration configurations (i.e., different well and WF types) [7], covering a V_T range of ~ 300mV (Fig. 4b). Well and WF types modulate the carriers distribution in the channel (Fig. 5a) with consequent impact on σI_D (Fig. 5b). Using n-well and n-WF, the carrier distribution is centered in the middle of the Si film. Thus, the current flow is less affected by interface defects located at the top oxide interface, with consequent noise performance reduction. The main contribution to the noise signal comes from the trapping/de-trapping events generated by defects located at the silicon channel-top gate oxide interface. To minimize D_{it} several gate oxide process improvements can be employed (Fig. 6a). The benefit directly translates into lower σI_D, evident in a more straight distribution (Fig. 6b). Different integration solutions can also be used to boost the device transconductance without affecting the interface quality. Fig. 7 shows the measured transconductance for a standard device and with specific integration elements (thin top oxide and thick silicon film) beneficial for g_m improvement without σI_D degradation.

4. Layout Optimization

FDSOI technology offers the unique possibility to modulate DC performance using back-bias (BG) capability. Constant BG is normally employed to tune V_T [7]. Back-bias impacts the noise performance as well [8]. Fig. 8 shows σI_D measured for different BG values. With negative back-bias, free carriers are pushed toward the top oxide interface with consequent σI_D degradation. Using positive BG, the carriers move toward the middle of the Si channel (i.e., minimum σI_D). With farther BG increase, the free carriers are confined close to the BOX with consequent σI_D degradation. Fig. 9 shows g_m/I_D versus I_D for a device with V_{BG}=0 and 2V. The two curves overlap. For analog application, where thick oxides are normally employed, superior intrinsic gain efficiency is obtained when front gate and back gate are acting together (inlet Fig. 9). The requirement is a balanced capacitor divider to utilize and maintain the effect. With BG=FG, a g_m/I_D improvement is shown especially in weak and moderate inversion area. The benefit directly translates in lower (i.e., better) noise performance. Hence, the gate voltage standard deviation ($\sigma V_T=\sigma I_D/g_m$) reduces with BG=FG for n-FET (Fig. 10) and p-FET (Fig. 11), respectively.

Conclusion

In this work we reviewed how device noise performances are strictly related to circuit operation point. Optimum trade-off between power efficiency and noise requirements must be found during design. Process integration can be optimized to further reduce noise of a single device. FDSOI technology offers the unique possibility to improve performance using back bias capability (BG=FG) without additional integration complexity.

References

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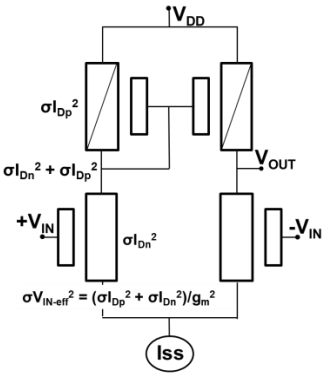

Fig. 1: Typical differential amplifier with n-FET and p-FET devices. Total noise contribution $\sigma V_{IN\text{-}eff}$ is affected by current fluctuations $\sigma I_{Dp,n}$ and device g_m.

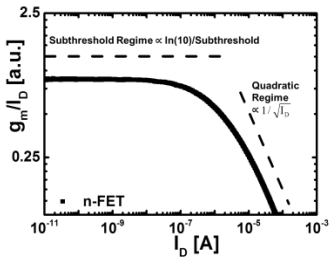

Fig. 2: g_m/I_D versus I_D for n-FET device. For different I_D set points, the device operates in different regimes.

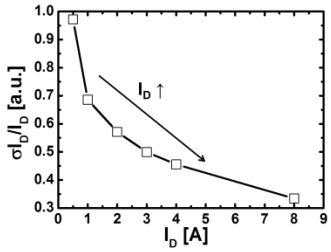

Fig. 3: $\sigma I_D/I_D$ versus I_D. Smaller noise contribution is evidenced for larger I_D. RTN measurement setup detailed in [9].

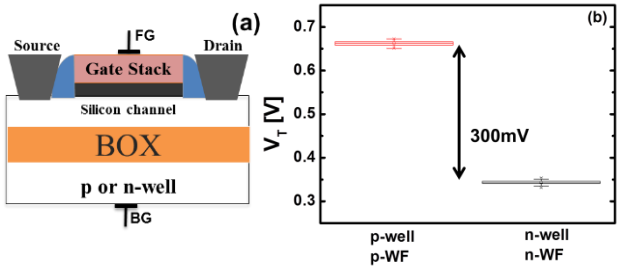

Fig. 4: (a) Schematic of FDSOI device layout. (b) V_T measured for n-Well, n-WF and p-Well, p-WF devices.

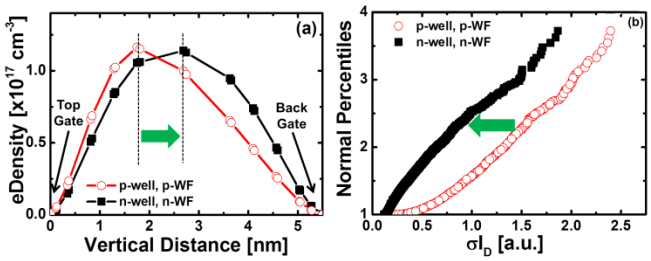

Fig. 5: Carrier distribution modulates noise. Lower σI_D is measured for n-well, n-WF devices thanks to the stronger immunity to interface traps due to free carriers distributed in the middle of the Si channel.

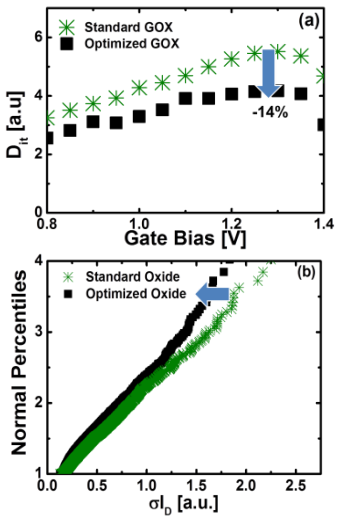

Fig. 6: Improved D_{it} with optimized gate oxide process GOX. The benefit directly translates in lower σI_D.

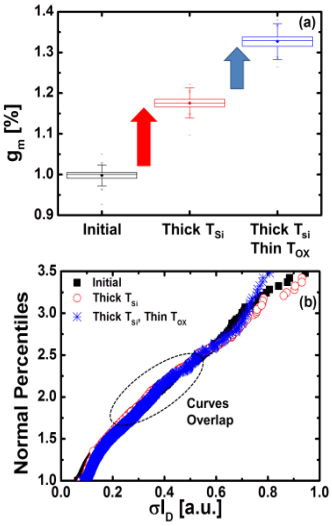

Fig. 7: g_m improvement with thick silicon film T_{Si} and thin top gate oxide T_{OX} without σI_D degradation.

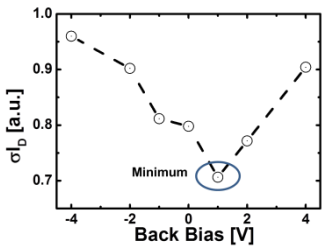

Fig. 8: Impact of back bias on σI_D. Minimum noise measured with light positive back bias. Measurements performed at constant current density.

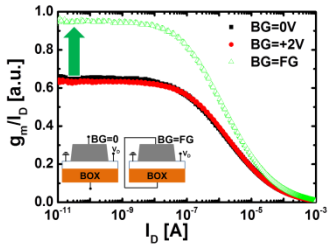

Fig. 9: g_m/I_D versus I_D for n-FET device using different BG. With BG=FG, significant g_m/I_D benefit at weak/moderate inversion.

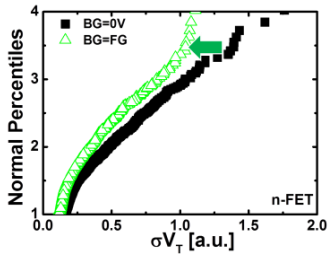

Fig. 10: n-FET σV_T reduction measured with BG=FG configuration.

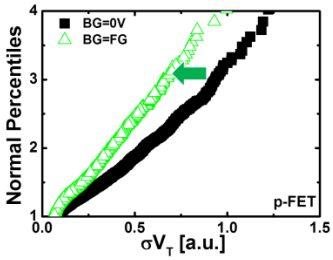

Fig. 11: p-FET σV_T reduction obtained with BG=FG configuration.