Impact of pFET channel formation and patterning on the strain in SiGe nanosheets investigated by µRaman spectroscopy

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Abstract- We fabricated SiGeOI and SiGe/SOI bilayer nanosheets down to 100nm width and investigated their strain by µRaman spectroscopy for different CMOS process integration schemes (of channel formation and patterning). We evidence experimentally a relaxation of the compressive strain in SiGe for narrow lines, which is higher for SiGeOI than for SiGe/SOI at W=500nm, in qualitative agreement with the electrical results we measured on planar FDSOI pMOSFETs. We highlight the interest of a tensile nitride capping on top of SiGe in order to maintain the stress during active patterning and demonstrate that a 0.45% tensile stress could be generated in 100nm narrow stripes in the underneath SOI layer of the SiGe/SOI bilayer thanks to a proper transfer of the SiGe stress. All of these results provide guidelines for stress and performance optimization in advanced planar FDSOI or nanosheets/nanowires CMOS devices.

Introduction-In advanced CMOS technologies, compressively-strained SiGe channels are highly efficient to boost the performance of pMOSFETs [1-3]. In such devices, electrical characteristics are strongly dependent on the active area dimensions [4,6]. This behavior, especially observed in SiGeOI <110>-oriented channel pFETs, was explained by a strain relaxation induced by the free edges created during the active patterning and evidenced by Nano-Beam Electron Diffraction (NBED) [4]. In this paper, we use uRaman spectroscopy in order to study the impact of different CMOS process integration schemes. Especially, we compare SiGe directly on insulator (SiGeOI) fabricated by condensation with a SiGe/SOI bilayer obtained directly by epitaxy. This specific study is partly motivated by the difference of electrical behavior, we measured, between SiGeOI and SiGe/SOI integrated as the channel of planar FDSOI pFETs in so-called "SiGe-first" or "SiGe-last" integrations, respectively [7]. The different threshold voltage evolution vs. the gate-to-STI distance SA for both samples/integrations illustrated in Fig.1 indeed suggests a difference of strain evolution at small dimensions.

Experiment- Different SiGe nanosheets have been fabricated. The reference process is the following: starting from a SOI substrate with a 6nm Si film and a 20nm-thin BOX, a 20nm-thin SiGe layer is grown by epitaxy with a targeted Ge concentration of 24%. Then, SiGe directly on insulator is obtained by a Ge-enrichment (so-called "condensation" step) at 1050°C (by Rapid Thermal Oxidation) [8]. The condensation oxide is then removed by wet etching. A 4nm-thick oxide pad and a 55nm-thick LPCVD SiN hard mask are deposited. A 30min anneal at $1050^{\circ}C$ under N₂ is then performed in order to allow Si and Ge atoms to inter-diffuse, resulting in a uniform SiGeOI layer. The stack is then patterned by UV lithography and an etching step with an end point in the substrate. The SiN hard mask is then removed by H₃PO₄. This reference sample (Fig.2a) is compared with other ones: with SiN (Fig.2c), without oxide pad (Fig.2d, an HF-last desoxidation is used to ensure that the SiN is deposited directly on the SiGe layer) and a SiGe/Si 'bilayer' sample (Fig.2b). The latter sample did not undergo

the condensation process neither the annealing.

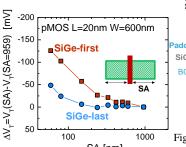
Our measurements were carried out using near-UV excitation wavelength λ =363.8nm from Ar+ laser, a 100x (numerical aperture=0.9) objective lens and a typical laser power of ~0.1mW to avoid any heating of the sample (penetration depth ~ few 10nm and spot diameter ~ 0.5µm). On each sample, the effective Ge concentration *x* was extracted by measuring the µRaman Si-Si peak frequency shift $\Delta \omega_{sisi}$ on a large active regions (assuming no plastic relaxation, eq.1 on Fig.3, [9]). The Ge concentration is found to be around 23% for all samples (Fig.5). Then, in order to compute the average perpendicular strain ε_{XX} from $\Delta \omega_{sisi}$ for narrow stripes, we have assumed that the strain parallel to the stripe is maintained (i.e. plane strain configuration, e_{YY} =0) and have used eq.5-6 (Fig.3).

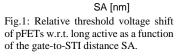
<u>Results and discussion-</u> Fig.4 shows the μ Raman spectra measured for the different SiGe samples and the extracted peak position in different regions: the SiGe layer, the Si substrate and, only for the SiGe/Si sample, the SOI layer (Fig.4d). Fig.6 summarizes the average perpendicular strain ε_{XX} extracted as a function of the stripe width. The compressive strain drops as the stripe width reduces. This can be explained by the free boundary condition at the edge of the stripe allowing a lateral relaxation. In order to confront the experimental data with theory, we have performed mechanical simulations in the elastic domain. For the SiGeOI sample, the experimental strain relaxation is higher than expected, whereas the SiGe/Si bilayer strain profile is closer to simulations. This suggests a specific mechanism of lateral relaxation in the patterned SiGeOI, which might be linked to the mechanical behavior of the BOX/SiGe interface after condensation. One way to manage the strain in the SiGe layer to be maintained is to keep the LPCVD SiN on top (Fig.6). This trend is qualitatively consistent with simulations and can be explained by a higher rigidity of the whole structure with SiN and by its 1GPa intrinsic tensile strain, which also tends to keep SiGe under compression (Fig.6). The integration of a pad oxide in-between the SiGe and the SiN does not change the picture (Fig.6).

Finally, in the case of the SiGe/Si, the width of the raw peak around 522.4 cm⁻¹ cannot be solely explained by the substrate signature but suggests a strained SOI layer (Fig.4). After extracting this component, we highlight a tensile strain generation in the Si layer below SiGe for narrow active. It is reproduced by mechanical simulations and can be explained by the relaxation of the SiGe layer, dragging the underneath SOI. This behavior is also of primary interest for future-node CMOS exploiting nanowires/nanosheets obtained from SiGe/Si stacks.

<u>Conclusion</u>. We have investigated the strain in SiGe nanosheets by μ -Raman spectroscopy after different steps of the CMOS process integration with a focus on the channel formation and active patterning. This study provides guidelines for strain optimization in advanced planar SiGe channel FDSOI and nanosheet / nanowire CMOS devices.

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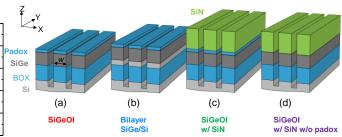


Fig. 2: Sketches of SiGe stripes of width w in the X direction [110] (not to scale). The stripes are 2mm long in the Y direction [1-10]. The vertical direction Z is oriented along the [001] direction. Four different stacks are investigated. (a) The reference condensed SiGe directly on insulator. (c) Same stack before SiN hard mask removal. (d) Same case as (c) but without pad oxide. (b) The SiGe/Si bilayer case, i.e. without condensation.

Pseudomorphic SiGe:	Uniaxial relaxation:
Lattice parameter: $a(SiGe)_{rel} = 5.431 + 0.2x + 0.027x^2$ (eq. 1)	$e_{XX} = (1 + \varepsilon_{XX}) \frac{a(SiGe)_{rel}}{a(Si)} - 1 $ (eq.5)
In-plane strain: $\varepsilon_{XX} = \varepsilon_{YY} = \varepsilon_{//} = \frac{a(Si) - a(SiGe)_{rel}}{a(SiGe)_{rel}}$; $\varepsilon_{ZZ} = -2\frac{C_{12}}{C_{11}}\varepsilon_{XX}$ (eq.2)	Relative deformation: $e_{YY} = (1 + \varepsilon_{//}) \frac{a(SiGe)_{rel}}{a(Si)} - 1 = 0$ Plane strain configuration
Out-of-plane relative deformation: $e_{ZZ} = \frac{(1 + \varepsilon_{ZZ})a(SiGe)_{rel} - a(Si)}{a(Si)}$ (eq.3)	$e_{ZZ} = \left(1 - 2\frac{C_{12}}{C_{11}}\left(\varepsilon_{XX} + \varepsilon_{//}\right)\right)\frac{a(SiGe)_{rel}}{a(Si)} - 1$
$\mu \text{Raman shift:} \Delta \omega_{SiSi} = \frac{1}{2\omega_0}, p, e_{ZZ} (eq.4) \qquad \Delta \omega_{SiSi} \implies \mathbf{x}, \mathbf{\varepsilon}_{//}$	$\Delta \omega_{sisi} = \frac{1}{2\omega_0} (q(e_{XX} + e_{YY}) + p.e_{ZZ}) (eq.6)$

Fig.3: Equations used for strain extraction according to μ Raman shift; *q* and *p* being the deformation potentials (*q*=-2.31 ω_0^2 *p*=-1.85 ω_0^2) [10-14] and a(SiGe)_{rel} the lattice parameter of fully relaxed SiGe.

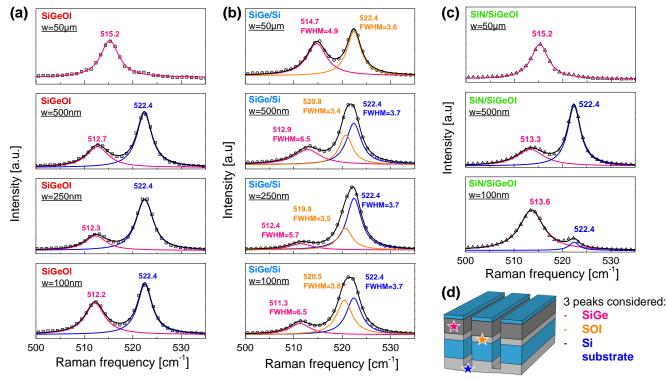


Fig.4: µRaman measurements focusing on Si-Si peak for (a) SiGeOI sample, (b) SiGe/Si bilayer sample, (c) SiN/SiGeOI sample and (d) illustration of the three peaks considered for fitting the experimental data with Lorentzian functions.

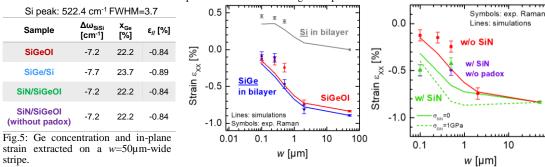


Fig.6: Strain perpendicular to the SiGe stripes extracted as a function of the stripe width from data shown in Fig. 4 for SiGeOI sample compared to (left) SiGe/Si bilayer sample and (right) SiN/SiGeOI sample. Lines are the results of mechanical simulations in the elastic domain.