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Introducing a highly efficient stressor for pMOS devices by controlling epitaxy and Ge enrichment in advanced planar FDSOI CMOS technology

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Abstract: In this work we study Germanium (Ge) enrichment in $Si_{(1-x)}Ge_x$ thin films for in-plane stress engineering in advanced FDSOI nodes. We detail in the following the different technological steps locally yielding in-plane compressive strain into the channel of UTBB devices. To that end, we used the so-called Self-Aligned In-Plane Stressor (SAIPS), an appealing architecture which was recently proposed as a solution to enhance carrier mobility. By introducing SiGe selective regrowth within state of the art 14nm FDSOI process, we report the highest compressive strain value (-1.1 GPa) achieved in SiGe UTBB devices.

1. Introduction

Current CMOS technological nodes [1] are at the heart of intense efforts with multiple architectures being proposed to improve performances at competitive costs. With a low process complexity and a good power consumption and performance tradeoff, Fully depleted planar devices (UTBB) are among the best candidates to introduce stressors in aggressively scaled technological nodes. A recent approach to such performance enhancement has been proposed in planar technologies. It consists in locally introducing uniaxial compressive stress in the sources/drains (S/D) regions of p-MOSFETs, the aim being to increase hole mobility in short gate length channels (SAIPS) [4][5][6]. FDSOI [2] is an outstanding platform to take advantage of such a concept. While [2][6] report on SAIPS application to Si-channel FDSOI, this technique was shown beneficial to SiGe channels [4]. In this paper, we discuss the process sequence that allows SAIPS performance enhancement in state-of-the-art SiGe pFET FDSOI devices.

The high Ge content SD regions at the core of SAIPS devices enable to tune the in-plane film stress. In a nutshell, higher Ge incorporation leads to higher in-plane compressive strain which results in hole mobility enhancement.
It was earlier reported through TCAD simulations that strains close to -1GPa should be achievable through the incorporation of approximatively 50% of Ge in SiGe stressors [7].
Using of a state of the art 300 mm CMOS integration flow (**Figure 1**), we focused on the Ge enrichment process, in order to inject controlled amounts of compressive strain in the channel underneath the gate. We then developed selective epitaxies of really high Ge content layers and investigated the epitaxial re-growth of lower Ge content SiGe:B layers on top.

2. Results

2.1 Experimental details

SiGe Selective Epitaxial Growth (SEG) was carried out in a commercial 300mm Applied Materiel Rapid Thermal CVD (RTCVD) reactor. The enrichment step was performed using a Rapid Thermal Oxydation (RTO) process. Oxide was removed thanks to HF diluted in water. Strain characterization was performed using Transmission Electron Microscopy (TEM) coupled with Precession Electron diffraction (PED).

2.2 Technology and process flow

The 14FDSOI STMicroelectronics technological platform was used to fabricate SiGe devices with local stress engineering (**Figure 2**). A nominal $L_g = 20nm$[2] and a 23% SiGe channel served as our base architecture.

2.2.1 SiGe selective Epitaxy

We developed a dedicated selective epitaxial regrowth process on the SiGe channel layer in order to enable SAIPS (**Figure 3**). Surface preparation, temperature control and selectivity optimization were key to keep the stack 2D and defects free for high Ge concentrations will be discussed.

2.2.2 Germanium enrichment

Based on previous simulations and experimental studies[3][4][7], two different Ge enrichment approaches are developed on the patterned wafers: the full enrichment (**Fig. 4a**) and the partial enrichment (**Fig. 4b**) processes. We employ a Rapid Thermal Oxidation to increase the Ge fraction on each side of the channel in S/D areas. Following SiGe epitaxial regrowth, Ge diffused during RTO towards the buried oxyde (Fig. 4) [4]. In the full enrichment case, we obtained a homogenous SiGe layer 44% in the <100> direction, this in the S/D regions and in the channel. In the partial enrichment case, we had SiGe 44% S/Ds on each side of the gate while keeping our SiGe 23% channel intact (Fig. 4).

2.2.4 Source/Drain re-growth

In order to allow a selective S/D SiGe35%:B epitaxial regrowth after enrichment, we had to optimize surface preparation and temperature control as we were operating on higher Ge content SAIPS layers than usual (44% vs 23%). We were successful as shown in (**Figure 3**).

2.2.5 Final results

Working on Epitaxy and Ge enrichment, we developed two approaches. The full Ge enrichment leads us to create a device on homogenous SiGe 44% channel starting from SiGe 23%. On the other hand, we demonstrate the benefit of a local Ge enrichment (partial Ge enrichment) in the S/D regions using the SAIPS technique. We archived a -0.8% compressive strain (**Figures 5 and 6**), i.e. a -1.1GPa uniaxial stress in the SiGe channel underneath the gate compare to the reference process flow.

3. Conclusions

This study performed in a CMOS manufacturing environment demonstrates that it is possible, with a few additional process, to boost the uniaxial compressive strain in advanced FD-SOI pMOSFETs. Increasing further the Ge content in the SiGe:B layers grown on top could be another key to further increase the embedded strain.

Acknowledgements

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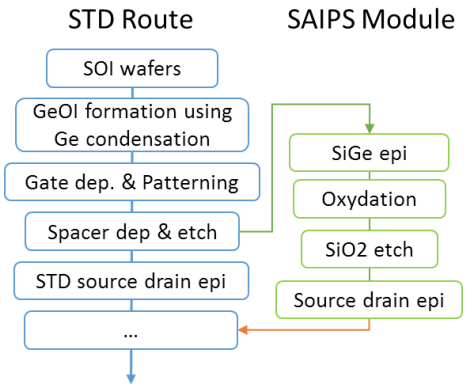

Figure 1: SAIPS Process Flow from STD

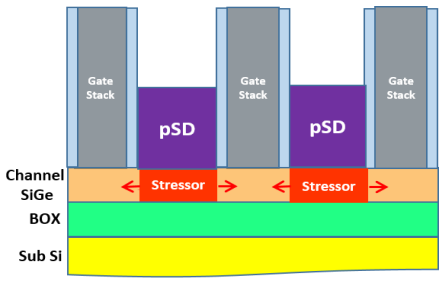

Figure 2: SAIPS architecture.

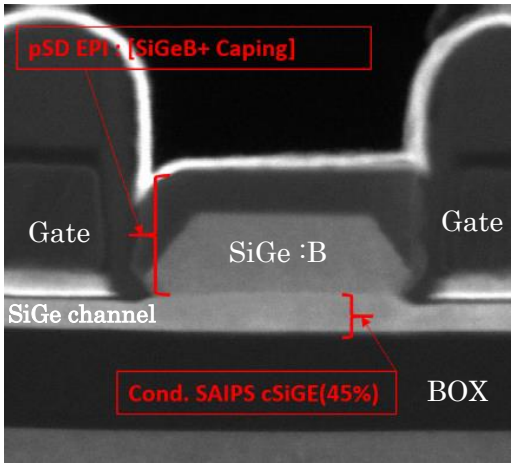

Figure 3: SiGe Epitaxial growth + Enrichment

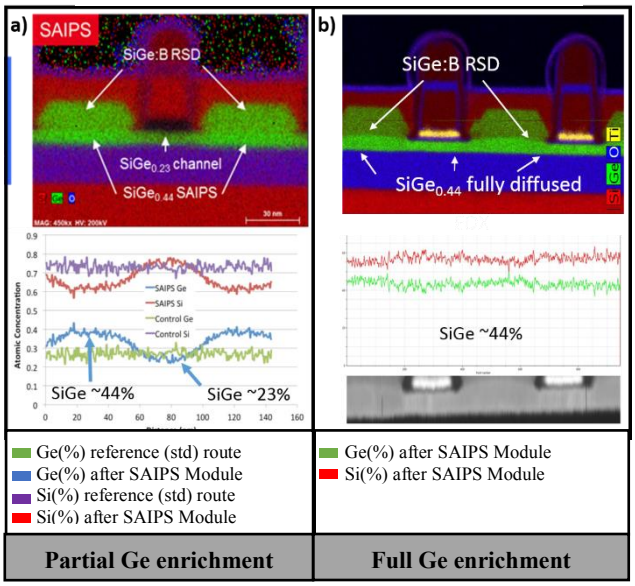

Figure 4: EDX after Ge enrichment and S/D regrowth

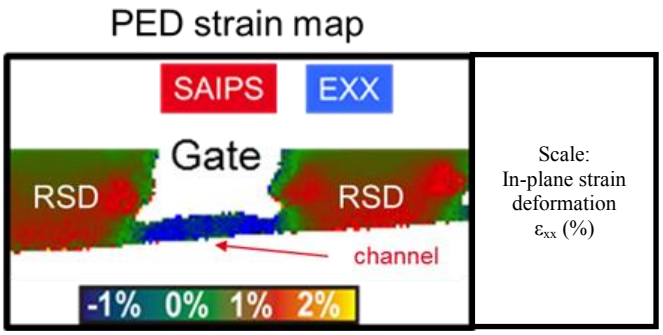

Figure 5: PED strain map after enrichment and S/D regrowth

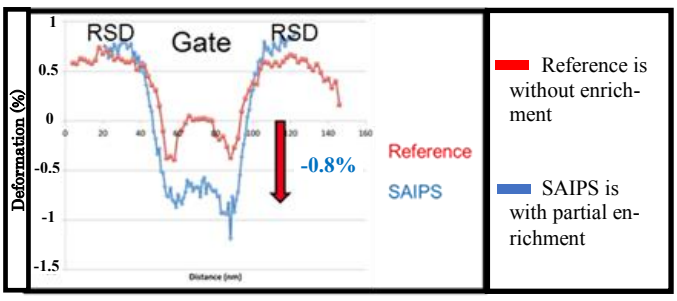

Figure 6: PED strain profile post enrichment and S/D regrowth