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Ge:B and GeSn:B Low Temperature Selective Epitaxial Growth Schemes for Source/Drain layers in Ge pMOS devices

A. Vohra[1, 2], C. Porret[2], D. Kohen[3], S. Folkersma[1, 2], J. Bogdanowicz[2], M. Schaekers[2], J. Tolle[3], A. Hikavyy[2], E. Capogreco[2], L. Witters[2], R. Langer[2], W. Vandervorst[1, 2], and R. Loo[2]

[1] K.U. Leuven, Dept. of Physics, Celestijnenlaan 200D, 3001 Leuven, Belgium
[2] Imec vzw, Kapeldreef 75, 3001 Leuven, Belgium
[3] ASM, 3440 East University Drive, Phoenix, AZ 85034, USA
Phone: +32-16-281404 E-mail: roger.loo@imec.be

Abstract

We report on production compatible low temperature (320°C) selective epitaxial growth schemes for boron doped $Ge_{0.99}Sn_{0.01}$ and Ge in source/drain areas of FinFET and Gate-All-Around strained Ge pMOS transistors. Active B concentrations are as high as $3.2x10^{20}$ cm^{-3} and $2.2x10^{20}$ cm^{-3} for $Ge_{0.99}Sn_{0.01}$ and Ge, respectively. The Ge:B growth is based on a cyclic deposition and etch approach while the $Ge_{0.99}Sn_{0.01}$:B growth is selective in nature. Low Ti/p+ Ge(Sn) contact resistivities (ρ_c) of $3.6x10^{-9}$ $\Omega.cm^2$ ($Ge_{0.99}Sn_{0.01}$:B) and $5.5x10^{-9}$ $\Omega.cm^2$ (Ge:B) have been obtained without using any post-epi treatment.

1. Introduction

The continuous downscaling of MOSFET devices leads to a reduction in Source/Drain (S/D) contact area which causes an increase in contact resistance (ρ_c), limiting device performances [1]. Novel approaches are required to significantly lower contact resistivity. In addition to high active doping, optimal S/D fabrication schemes need to provide conformal epi layers, grown with a restricted thermal budget (preferentially without thermal treatments for doping activation) without compromising the material crystalline quality. In addition, the grown layers should be thermally stable and have a lattice constant suitable to introduce the correct strain type in the channel. For Ge pMOS devices the low boron solubility in Ge ($5.5x10^{18}$ cm^{-3}) is a major challenge [2]. For Ge, novel low temperature epitaxial growth schemes aimed at increasing the active dopant incorporation are often based on attempts to move the growth process as far as possible away from equilibrium [3-5]. The use of Ge_2H_6, for instance, allows to reduce the growth temperature, while still maintaining material quality and an acceptable growth rate which helps to boost active doping incorporation [3,4]. However, owing to its non-selective nature, the epi process requires the use of deposition-etch cycles for the selective growth of S/D on device wafers. Margetis et al. reported the epitaxial growth of in-situ doped GeSn using GeH_4 and $SnCl_4$ as Ge and Sn precursors, respectively [5]. The incorporation of Sn acts as a catalyzer enabling *selective* epitaxial growth at low growth temperatures thereby enabling active boron concentrations up to 2×10^{20} cm^{-3} [5] which can be further increased to 5×10^{20} cm^{-3} for δ-doped GeSn [6]. Because of the low Sn solubility in Ge, implementation on narrow fins is challenging as there is a high risk for Sn agglomeration in confined volumes.

In this work, we introduce low temperature *in-situ* B-doped $Ge_{1-x}Sn_x$ and Ge Chemical Vapor Deposition (CVD) processes meeting the above mentioned requirements for S/D stressors. Enhanced active boron concentrations of $3.2x10^{20}$ cm^{-3} ($Ge_{0.99}Sn_{0.01}$:B) and $2.2x10^{20}$ cm^{-3} (Ge:B) have been achieved with ρ_c down to $3.6x10^{-9}$ $\Omega.cm^2$ ($Ge_{0.99}Sn_{0.01}$:B) and $5.5x10^{-9}$ $\Omega.cm^2$ (Ge:B) without any *post-epi* anneal. We will demonstrate fully selective epitaxial growth in S/D areas of FinFET and Gate-All-Around (GAA) strained Ge device structures. In current Ge pMOS devices, channel strain is based on the use of SiGe strain relaxed buffers, and the chosen S/D materials introduce the preferred compressive channel strain to boost carrier mobility.

2. Experimental

$Ge_{1-x}Sn_x$:B and Ge:B layers were epitaxially grown by CVD on blanket Ge virtual substrates (VSs) using a 300 mm production compatible ASM Intrepid XP™. $Ge_{1-x}Sn_x$:B layers were grown with conventional gas precursors (GeH_4, $SnCl_4$, and B_2H_6). Optimized $Ge_{1-x}Sn_x$:B growth conditions for the highest active doping concentration and the lowest ρ_c as obtained on blanket layers, were used as starting conditions for $Ge_{1-x}Sn_x$:B growth on relaxed Ge FinFET patterned wafers with fin widths ranging from 10 to 100 nm. Process conditions were adjusted to suppress Sn precipitation & loading effects and to maintain material quality. The growth behavior was then confirmed using FinFET patterned wafers containing strained $Ge/Si_{0.35}Ge_{0.65}$ multilayers on top of $Si_{0.3}Ge_{0.7}$ strain relaxed buffers (SRBs) as used for GAA devices [7]. Ge:B layers were grown with Ge_2H_6 instead of GeH_4. For the growth on patterned wafers we developed a cyclic deposition-etch (CDE) routine using Cl_2 as etchant. Both methods facilitate increased growth rates at reduced growth temperatures (< 350°C). Contact resistivities were extracted from multi-ring circular transmission line model (MR-CTLM) structures using the fabrication scheme described in [8,9]. Active doping concentrations have been measured by micro-Hall effect measurements [10] assuming a Hall scattering factor of 1.

3. Results and Discussion

Exceeding boron solubility in Ge by a factor 60 through Sn alloying

The maximum active boron concentrations which can be achieved in Si, $Si_{1-x}Ge_x$ and Ge are typically obtained for $Si_{1-x}Ge_x$ with 40-70% Ge (Fig. 1) [7]. However, Ge pMOS devices require S/D layers with a larger lattice constant i.e. pure Ge. For Ge growth with GeH_4, we reached an active doping

concentration of $3x10^{19}$ cm^{-3}, which is exceeding the B solubility limit by approximately a factor 5 (Fig. 1). Higher active doping concentrations are obtained by using Ge_2H_6 as precursor gas (~ $2x10^{20}$ cm^{-3}) or by Sn alloying ($3.2x10^{20}$ cm^{-3}) (Fig. 1). For GeSn, a high material quality is confirmed by HR-XRD. SIMS measurements confirm a constant B profile as function of depth. With increasing B_2H_6 partial pressure, Sn incorporation reduces [5,6] but this has no detrimental effect on growth rate [11].

ρ_c values of $3.6x10^{-9}$ $\Omega.cm^2$ and $5.5x10^{-9}$ $\Omega.cm^2$ are extracted from Ti/$Ge_{0.99}Sn_{0.01}$:B and Ti/Ge:B stacks, respectively. These ρ_c values have been obtained without post-growth thermal treatments to increase active dopant concentration.

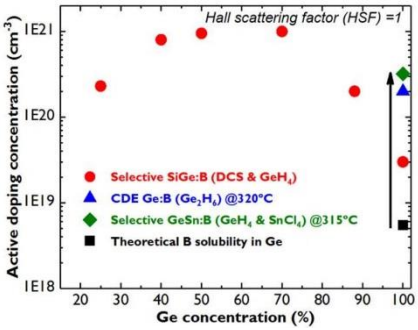

Fig. 1 Highest active boron concentrations in Si, SiGe, Ge and GeSn as measured by μHall measurements using processing conditions which enable selective epitaxial growth.

Growth characteristics on patterned fins

Loading effects result in an enhanced Sn and B incorporation when the process conditions as developed for epitaxial $Ge_{1-x}Sn_x$ growth on blanket Ge virtual substrates are used on device patterned wafers. For the given mask-set with an open Si area of 60.1%, it results in 4x higher growth rates, significant Sn agglomeration (Fig. 2a) and B precipitation. EDX measurements confirm that the 'bubbles' seen in Fig. 2a are Sn-enriched. Consequently, the $SnCl_4$ partial pressure need to be adjusted to avoid Sn agglomeration (Fig. 2b).

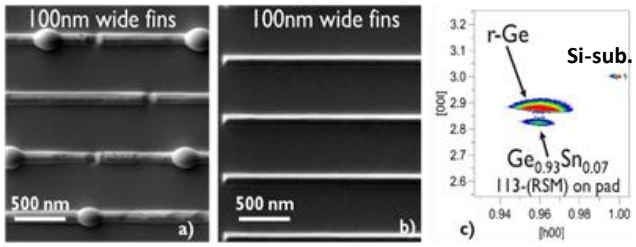

Fig. 2: a, b) Top-view SEM showing undoped $Ge_{1-x}Sn_x$ epitaxially grown on relaxed-Ge 100 nm wide fins. a) Process conditions as used for blanket wafers result in Sn agglomeration. b) Optimized process conditions result in smooth $Ge_{0.93}Sn_{0.07}$ surfaces. c) RSM measurement of the layer shown in figure b) but taken on 80x80 μm^2 test structures (same wafer).

For the given example, Reciprocal Space Mapping taken on 80x80 μm^2 test structures indicates that the $Ge_{1-x}Sn_x$ is fully strained and that the Sn content is ~ 7% (Fig. 2c). Following Sn content adjustment, the B_2H_6 partial pressure is optimized to obtain the highest B incorporation without any surface morphology degradation. Fig. 3a shows an example of a $Ge_{0.99}Sn_{0.01}$:B layer epitaxially grown on the S/D areas of a fin-patterned Ge/SiGe multi-stack as used for GAA devices. μHall measurements on 80x80 μm^2 test structures confirm an active boron concentration of $2x10^{20}$ cm^{-3}.

The Ge:B CDE process relies on the selective etch of amorphous and polycrystalline materials vs crystalline counterparts. As the Ge deposition is non-selective, it does not suffer from loading effects. As a result, transferring the growth conditions to patterned wafers is relatively straighforward, provided that the structural properties of the monocrystalline S/D regions are maintained. Fig. 3b confirms the full selectivity of the process versus the SiO_2 shallow trench isolation and nitride spacers. It also indicates that the S/D material quality is sufficiently high as the selective etching does not result in any observable etch pits nor roughness.

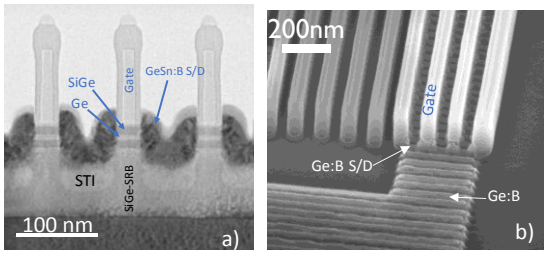

Fig. 3. a) Cross-section TEM of GeSn:B selectively grown on S/D areas of strained-Ge/SiGe multi-stack as used for Ge GAA devices. b) Tilted-view SEM of a Ge:B grown by CDE on relaxed Ge fins with gate patterning

4. Conclusions

Selective, *in-situ* B-doped epitaxial $Ge_{0.99}Sn_{0.01}$ and Ge with high dopant activation and low ρ_c was achieved without any post-epi anneal. Either Sn-alloying or using Ge_2H_6 as precursor gas offer higher growth rates at a lower growth temperature, thereby enabling an increase in maximal achievable active doping. For both schemes we demonstrated fully selective growth in S/D areas of FinFET patterned device structures. For $Ge_{0.99}Sn_{0.01}$, a careful optimization of process conditions is required to suppress Sn precipitation and degradation of material quality, while for the growth of Ge:B with Ge_2H_6, a cyclic deposition-etch approach is required.

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