Extended Abstracts of the 2018 International Conference on Solid State Devices and Materials, Tokyo, 2018, pp181-182

Sub-60mV/dec Subthreshold Swing on Reliability of Ferroelectric $HfZrO_x$ Negative-Capacitacne FETs with DC Sweep and AC Stress Cycles

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Abstract

The proposed 5nm-thick ferroelectric $Hf_{1-x}Zr_xO_2$ (FE-HZO) FET with sub-2.3k_bT/q is demonstrated on reliable stability for NC operation. A gradual transition of ferroelectricity with crystallization temperature increasing results in subthreshold swing (SS) < 60mV/dec and hysteresis loop formation. The superior stability of FE-HZO is validated with DC sweep for 100 times and AC stress for 10^6 cycles, exhibiting SS_{rev}=40-60mV/dec. It is promising to use ultra-thin FE-HZO as the guidelines for NC applications.

1. Introduction

The ferroelectric material with bi-stable potential state feature to storage energy satisfies the demands of voltage amplification concept for negative capacitance (NC) [1][2]. ZrO2 and HfO2 with supercycle for $Hf_{1-x}Zr_xO_2$ as gate stack has been intensively and extensively investigated to integrate with FETs due to following current CMOS architectures and feasibility ALD (atomic layer deposition) [3][4]. Recently, nearly equal mole ratio mixture of Zr and Hf after metal capping and annealing for ferroelectric transition demonstrates NC effect for steep-slope FET (SS-FET) [5-7]. The reliability issue of NC-FETs may be concerned with fatigue operation in order to implement future technology node. In this work, the reliability is discussed by multiple DC and AC pulse sweep to obtain SS sub-2.3k_bT/q.

2. Devices Fabrication

Process flow of the baseline Ferroelectric $HfZrO_x$ FETs with gate-last process is shown in Fig. 1. First the Source/Drain region is defined after wafer clean, and followed by ion implantation. The 1000°C spike annealing for dopant activation by RTA (Rapid Thermal Annealing) is carried out. Thin films of HZO are grown by ALD on Si substrate, and then the 120-nm-thick TaN is covered on the prior insulator layer by a sputtering system sequentially. The diode area is then defined by photolithography and etched by RIE to form the MESA structure. The annealing process for the crystallization of HZO is performed by RTA in an Ar ambient for 30 sec.

3. Results and discussion

The typical ferroelectric characteristics of MFM (metal/ferroelectric/metal) with HZO 10 nm shows typical hysteresis loop with different applied voltage from 1V to 3.4V and with different operation frequency as shown in Fig. 2(a). The hysteresis loop spreads out with applied voltage higher than 1.6V and saturates at 2.6V in MFM with 10nm HZO. This is one of ferroelectric characteristics for complete dipole switching beyond coercive voltage [8]. Figure. 3 shows the as-fab. 5nm HZO with SS>60mV/dec and clockwise direction in V_T shift for reverse sweep, which is the typical dielectric high-K behavior. The V_T shift becomes small and SS is also improved until 500°C annealing. The drain current floor is also improved due to the recovery of the interface trap. The counterclockwise direction of sweep and SS_{rev}<60mV/dec is obtained due to NC effect after 600°C annealing. This leads crystallization formation for ferroelectricity and makes the gate leakage current path along the grain boundary to obtain the drain current floor higher. The gradual transition in SS and V_T shift of 5nm HZO can be realized by well Source/Drain activation. The reliability issue of NC-FETs may be concerned with fatigue operation in order to implement future technology node. Figure. 4 shows the transfer characteristics ($I_{DS}V_{GS}$) of FE-HZO (ferroelectric-HZO, annealed) FET with multiple DC sweep (1000 times). The drain current and SS degradation is occurred. Figure. 5. shows the SS vs. DC sweep times. Note that DE-HZO denotes dielectric-HZO, which is un-annealed HZO. The FE-HZO FET exhibits high sustainability until 100 times DC sweep cycles on SS and keeps SS_{rev} < 60mV/dec. After 100 times DC sweep, the FE-HZO FET seems degradation. Besides, the AC stress with triangular waveform is performed on FE-HZO FET as shown in Fig. 6. for periods 4ms. The stress voltage is bipolar ±2V to emulate fast sweep operation. The transfer characteristics of FE-HZO FETs exhibits high stability with AC operation as shown in Fig. 7, indicating that the dipole switching under ±2V for 5nm may not induce extra defect formation. There is no significant current degradation for 5nm FE-HZO FET after 10^6 cycles with frequency 1/4 kHz AC stress. The SS exhibits 40-60 mV/dec for initial and after AC stress. Besides, the high-speed operation may induce higher E_c (Fig. 2(b)) and increase displace current to lead SS and ΔV_T improvement with more dipole switching.

4. Conclusions

The superior stability of FE-HZO is validated with DC sweep for 100 times and AC stress for 10^6 cycles, exhibiting SS_{rev}=40-60mV/dec. It is promising to use ultra-thin FE-HZO as the guidelines for NC applications. The proposed 5nm-thick ferroelectric $Hf_{1-x}Zr_xO_2$ (FE-HZO) FET with sub-2.3k_bT/q is demonstrated on reliable stability for NC operation.

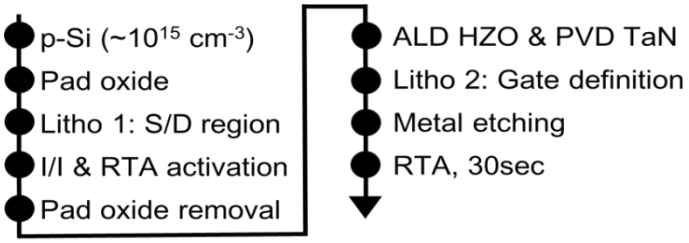

Fig. 1. The process flow of the baseline Ferroelectric $HfZrO_x$ FETs with gate-last process.

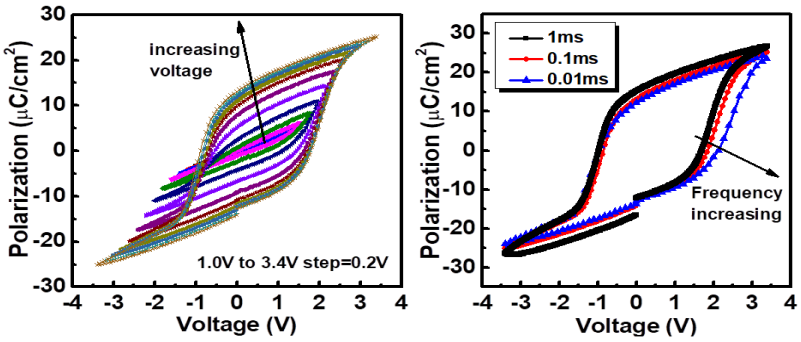

Fig. 2. The typical ferroelectric characteristics of MFM (metal/ferroelectric/metal) with HZO 10 nm. (a) Hysteresis loop with different applied voltage from 1V to 3.4V. (b) Hysteresis loop with different operation frequency. The related reliability discussion of ferroelectric HZO FET in this work is based on the typical characteristics.

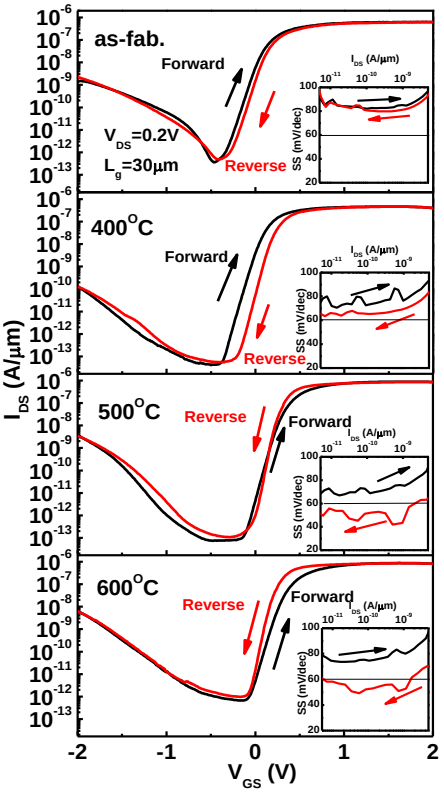

Fig. 3. $I_{DS}V_{GS}$ of 5nm HZO for as-fab, and annealing at 400°C, 500°C & 600°C. The as-fab. 5nm HZO shows SS>60mV/dec and positive V_T shift for reverse sweep, which is the typical dielectric high-K behavior. The counterclockwise direction of sweep and SS_{rev}<60mV/dec is obtained due to NC effect after 600°C annealing.

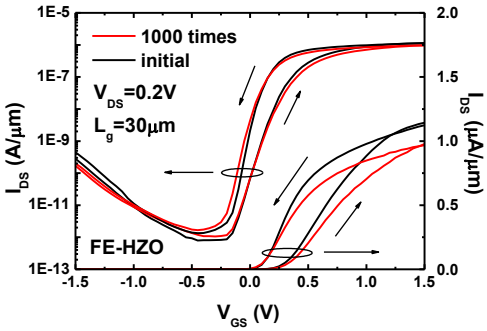

Fig. 4. $I_{DS}V_{GS}$ of 5nm FE-HZO with multiple DC sweep (1000 times). The drain current and SS degradation is occurred.

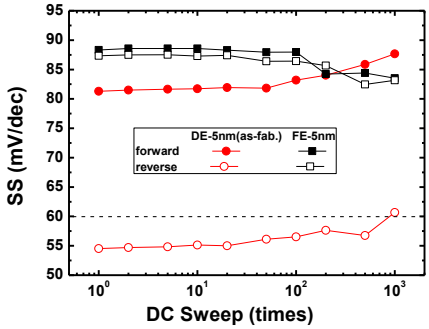

Fig. 5. SS of 5nm DE-HZO and FE-HZO with multiple DC sweep. The FE-HZO FET exhibits high sustainability until 100 times.

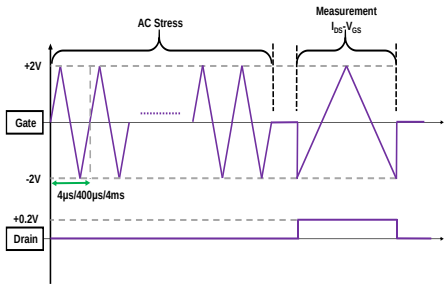

Fig. 6. AC stress with triangular waveform for periods 4ms. The stress voltage is bipolar ±2V to emulate fast sweep

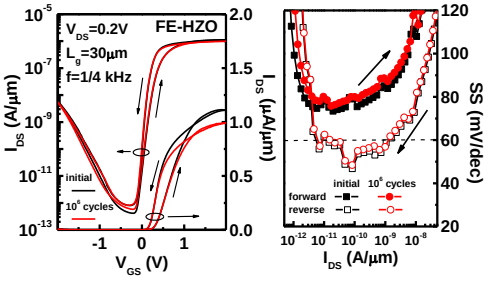

Fig. 17. (a) $I_{DS}V_{GS}$ and (b) SS vs. I_{DS} of 5nm FE-HZO with AC stress cycles. There is no significant current degradation for 5nm FE-HZO FET after 10^6 cycles with frequency 1/4k Hz AC stress. The SS exhibits 40-60 mV/dec for initial and after AC stress.

Acknowledgments

The authors are grateful for the funding support from the National Science Council (MOST 105-2628-E-003-002-MY3 & MOST 106-2221-E-003-029-MY3 & MOST 105-2622-8-002-001), process supported by National Nano Device Laboratories (NDL) & Nano Facility Center (NFC), Taiwan.

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