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Impact of channel thickness fluctuation on performance of bilayer tunneling field effect transistors

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Abstract

Impact of channel thickness fluctuation (CTF) on electrical characteristics of bilayer TFETs has been investigated on a basis of TCAD simulation and AFM analysis. Degradation of the sub-threshold properties of I_d-V_g characteristics of the bilayer TFETs by CTF is quantitatively examined, highlighting the importance of improvement in channel thickness uniformity. In addition, benefits of EOT scaling to ensure the potential of the bilayer TFETs have been clarified.

1. Introduction

A bilayer tunneling field effect transistor (TFET) with a gate-normal band-to-band tunneling (BTBT) has been actively studied, since it is a suitable structure to realize both extremely small sub-threshold swing (*SS*) and sufficient ON-state current (I_{ON}) [1-3]. Recently, we have proposed and succeeded the experimental demonstration of the bilayer TFET by utilizing the hetero-tunneling junction of an n-type oxide semiconductor (n-OS) and a p-type group-IV semiconductor (p-IV) with type-II energy band alignment (Fig. 1) [4]. This newly proposed TFET also allows us to provide high CMOS compatibility thanks to the simple device structure and fabrication processes.

On the other hand, there is a large gap between the theoretically expected performances and the experimental results [4]. One of the possible reasons is non-uniformity of the channel layer, which is composed of a PLD-deposited n-OS channel layer. This is because it can cause non-uniformity of BTBT over the channel region, which can be a common challenge for high-performance bilayer TFETs. Therefore, in this study, we investigate the influences of the channel thickness fluctuation (CTF) on the bilayer TFET performance. Furthermore, we show the impact of EOT scaling on performance degradation by CTF to ensure the high potential of the bilayer TFETs.

2. Results and discussion

2-1. Experimental evaluation of CTF

Fig. 2 shows cross sectional TEM images of the tunneling junction and an AFM image of the ZnO layer surface. A columnar-shaped poly-crystalline ZnO layer is observed. In addition, relating to the ZnO grain formation, the ZnO layer surface is fluctuated. Fig. 3 shows the histogram of the ZnO surface roughness obtained from the AFM image, which is the basic information to examine the influence of CTF in this study. Since the interface between the ZnO layer and Si substrate is smooth, this fluctuation directly corresponds to CTF in the fabricated TFET. The main portion of the distribution can be fitted by Gaussian with a standard deviation (σ) of 0.58 nm, while the distribution has a tail in the larger height (thickness) side.

2-2. Influence of CTF

The influence of channel thicknesses (t_c) on the I_d-V_g characteristics of the bilayer TFET has been evaluated by Sentaurus TCAD simulation (Fig. 4). EOT used here is 4 nm [4], and the carrier concentrations in the n-ZnO channel and the p-Ge source are assumed to be 3×10^{18} and 5×10^{18} cm^{-3}, respectively. With increasing t_c, V_{OFF} (I_{OFF} = 10^{-7} μA/μm) shifts to the negative V_g side and I_{ON} exponentially decreases, which are due to the larger band bending of the n-OS channel and the longer tunneling distance, respectively. It is noted that the sub-threshold swing of I_d-V_g is not degraded so much by thicker or thinner channels. However, since t_c is fluctuated in one device in the realistic situation, the total I_d-V_g curves becomes less steep as a result of the summation of multiple I_d-V_g curves with different V_{OFF} (Fig. 5).

Fig. 6 shows the I_d-V_g characteristics calculated by using CTF based on the AFM result, as introduced in Fig. 5. Since V_{OFF} is negatively shifted by CTF, the sub-threshold properties are degraded. The averaged *SS* in several operating conditions with fixed I_{OFF} of 10^{-7} μA/μm is found to increase with CTF, as summarized in Fig. 7. It is also observed from the comparison between two CTF distributions, Gaussian fitting and AFM histogram, shown in Fig. 3, that the tail of the fluctuation leads to the further degradation of *SS*. Additionally, at a certain V_g swing of 0.1 or 0.3 V aiming for the low power device operation, the obtainable I_{ON} is reduced largely due to the negative V_{OFF} shift (Fig. 8). These results emphasize the necessity of improvement of the t_c uniformity for the better performance.

2-3. Benefit of EOT scaling

In our previous study, it has been found that there is no clear benefit of EOT scaling on the sub-threshold properties of the TFET without CTF [4]. On the other hand, if CTF in the TFET is not negligible as discussed above, EOT scaling can be an effective way to mitigate the influences of CTF, leading to the enhancement of the TFET performance. Fig. 9 clearly shows that EOT scaling increases I_{ON} and suppresses the V_{OFF} shift caused by CTF, realizing the better sub-threshold property. Fig. 10 benchmarks the impacts of EOT scaling on bilayer TFETs with CTF. In thicker EOT, the average *SS* increases and I_{ON} decreases because of the CTF effect. Meanwhile, the average *SS* under EOT scaling hardly increases even under the same amount of CTF. Also, EOT scaling increases I_{ON} with suppressing its degradation with CTF. As a result, EOT scaling as well as improvement of t_c uniformity are important directions to improve the bilayer TFET performance.

3. Conclusions

In this study, we have investigated the influences of CTF on the electrical characteristics of bilayer TFETs with vertical BTBT, based on TCAD simulation and the AFM analysis. The numerical analysis indicates that V_{OFF} of the I_d-V_g curves is negatively shifted by CTF, leading to the *SS* increase and I_{ON} reduction. It is also clarified that not only improvement in t_c uniformity but also EOT scaling are critical issues to maximize the performance of the bilayer TFETs.

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References: [1] L. Lattanzio *et al.*, IEEE Elec. Dev. Lett. **33**, 167 (2012). [2] C. Hu *et al.*, Tech. Dig. IEDM 2010, p.387. [3] D. Sarkar *et al.*, Nature **526**, 91 (2015). [4] K. Kato *et al.*, Tech. Dig. IEDM 2017, p.377. [5] K. Kato *et al.*, Appl. Phys. Lett. **112**, 162105 (2018).

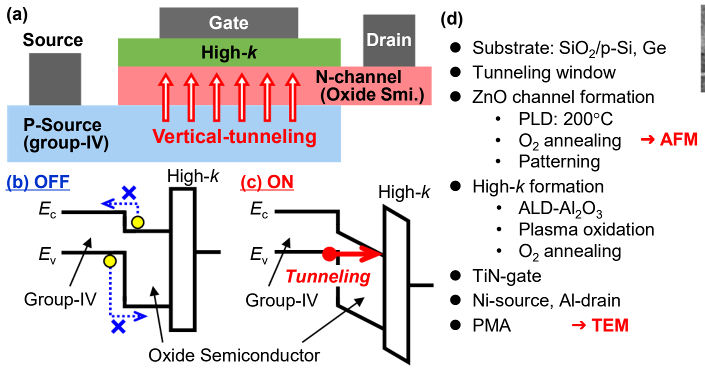

Fig. 1 (a) device structure image and energy band diagrams in (b) OFF state and (c) ON state, respectively. (d) Typical device fabrication flow with PLD ZnO channel deposition and engineered gate stack formation [5].

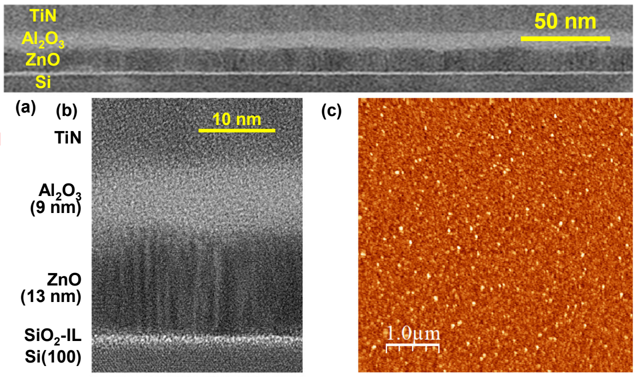

Fig. 2 (a) and (b) cross-sectional TEM images of tunneling junction and (c) AFM image of ZnO surface. Columnar poly-crystalline ZnO layer with thickness fluctuation is observed.

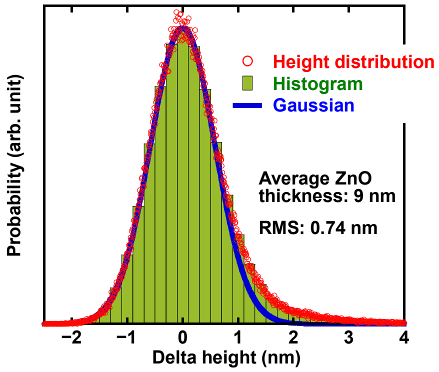

Fig. 3 Height histogram of ZnO surface obtained from the AFM image.

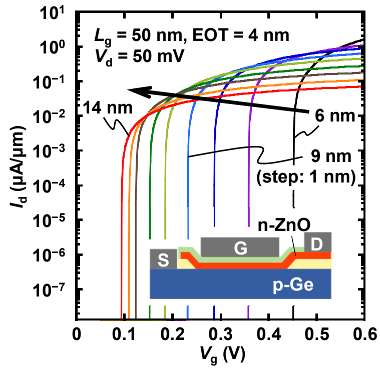

Fig. 4 Change in I_d-V_g characteristics of ZnO/Ge TFET with ZnO channel thickness.

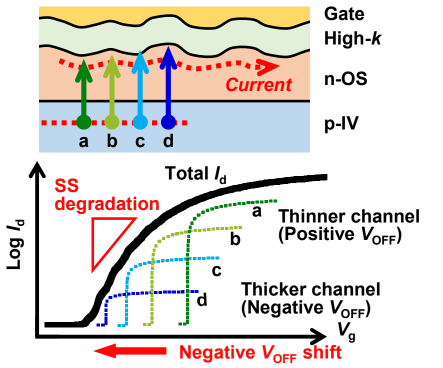

Fig. 5 Schematic illustration of degradation of TFET I_d-V_g characteristic caused with CTF.

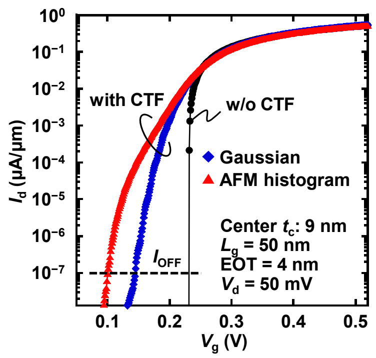

Fig. 6 Degradation of TFET I_d-V_g with CTF. Two CTF distributions, Gaussian fitting and AFM histogram (Fig. 3), are assumed.

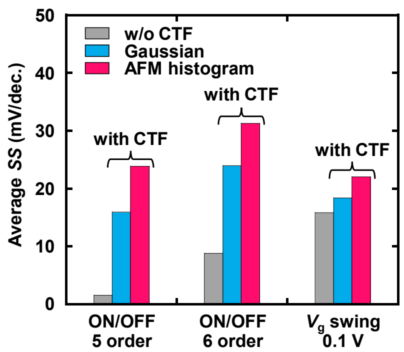

Fig. 7 Degradation of average SS with CTF in several operation conditions. The fixed I_{OFF} of 10^{-7} μA/μm is used.

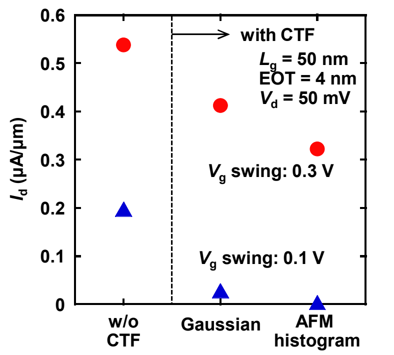

Fig. 8 Decrease in I_d with CTF at a certain V_g swing of 0.1 or 0.3 V.

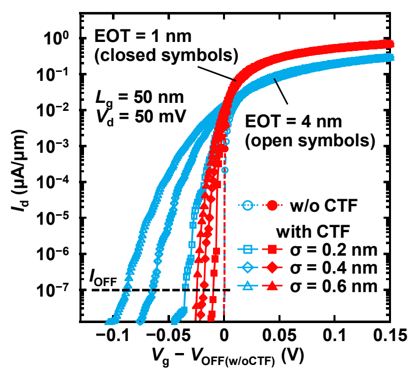

Fig. 9 Difference in degradation of TFET I_d-V_g with CTF for EOT of 1 and 4 nm.

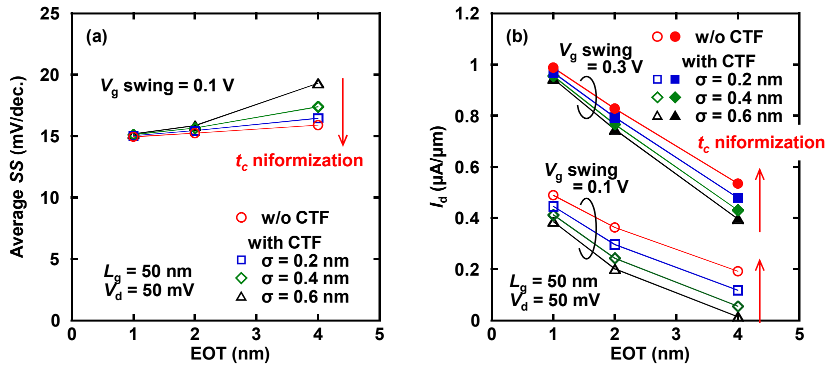

Fig. 10 Impacts of EOT scaling on bilayer TFET with and without CTF; (a) average SS with V_g swing of 0.1 V and (b) I_d at V_g swing of 0.1 or 0.3 V.