Extended Abstracts of the 2018 International Conference on Solid State Devices and Materials, Tokyo, 2018, pp189-190

A Novel Experimental Approach to Extracting Negative Capacitances: Newly found Negative DIBL Effect in 14nm NC-FinFET and the Way to Achieve Hysteresis-free

Y. C. Luo[1], E. R. Hsieh[2], C. J. Su[3], Steve S. Chung[2], T. P. Chen[4], S. A. Huang[4], T. J. Chen[4], and Osbert Cheng[4]
[1]*Department of Electrical Engineering, National Tsing Hua University, Taiwan,* [2]*Department of Electronics Engineering, National Chiao Tung University, Taiwan, Taiwan,* [3]*National Nano Device Laboratories(NDL), Taiwan,* [4]*United Microelectronics Corporation (UMC), Taiwan*

Abstract- *For the first time*, we have developed experimental approaches to quantitatively extracting negative capacitance and revealing a new negative DIBL effect in NC- FinFET. From this method, the growth mechanism of ferroelectric HZO can be well explained. It was found that DIBL with NC effect decreases along with the increase of V_{ds}. Furthermore, we found σV_t dramatically reduced with NC effect in addition to the S.S. reduction. For body effect, in the presence of NC effect, NC effect increases sensitivity so that hysteresis of NC-FinFET can be eliminated. In addition to a steeper SS of NC-FinFET, our work has proven that by suitably choosing body bias, NC-FinFET can not only help to improve the short-channel effect but also exhibit hysteresis-free, which makes it more applicable in low-power and high-performance apps in the future.

1. Introduction

NC-FET has become one of the most promising low-power transistors with high performance in IoT and HPC. NC-FET offers steep SS(< 60mV/dec) experimentally[1-3]. Nano- fabrication which NC-FETs require is compatible with that of the mainstream FinFET technology [4-5]. However, the negative capacitance values have not been quantitatively characterized till now although NC behavior can be indirectly observed in SS or CV. Furthermore, in addition to NC effect, a ferroelectric thin film is usually accompanied by a hysteresis, which increases tremendous complexity to circuit designs [2, 6]. In this work, we aim to develop an experimental approach to directly extracting NC values and examining the short-channel and body effects of an HZO MIM gated FinFET, from which zero hysteresis operation of NC-FET can be achieved. The experimental methods will also be used to extensively investigate the σV_{th}, SS, DIBL, I_{off}, and body sensitivity on the fabricated 14nm HZO-gated FinFET. The results in this work will provide very valuable on understanding more device physics of NC effect so as to design appropriate electrical characteristics of NC-FinFET.

2. Device Preparation

TiN/HZO(9nm)/TiN samples whose area= 100μm^2 were prepared in annealing temperature from 400^{0}C to 700^{0}C. The FinFET is based on the UMC 14nm technology platform. MIM is then electrically connected to the gate of 14nm-nFinFET with W/L=1/0.1 (μm) for the whole measurement. (Fig.1)

3. Results and Discussions

A. Approaches to Experimentally Extracting NC Values

Fig. 1 is the experimental setup. When V_{gs} is applied on MIM, HZO will modulate the channel carriers of the transistor. In the presence of NC-effect, it is assumed that effective negative capacitance(C_{NC}) will be serially connected to HZO MIM cap(C_{HZO}). In Fig. 2, we observe flip-flops of bulk dipoles in an HZO MIM. Before voltage sweeps, bulk dipoles are randomly distributed. But, as external bias is across MIM, bulk dipoles will be aligned in an opposite direction to this external field. As a result, a built-in field of dipoles is polarized and induces NC effect. From this observation, we expect NC effect appears during the backward sweep but not for the forward one. Therefore, in a gated HZO-FinFET, Fig. 1, we should observe corresponding forward and backward routes of I_dV_{gs} as in Fig. 3. The forward route of Fig.3 is I_dV_{gs} without NC effect, while the backward is I_dV_{gs} with NC effect, from which we see the hysteresis. It should be noted that NC effect from HZO only affects C_{ox} of nFinFET; hysteresis just influences V_t, and μ_{eff} will not respond to remote scattering events from HZO because of filed-screening from gate metals. Therefore, we extract C_{NC} in HZO MIM by the derivations in Table 1. In Fig. 4, it is of interest to find that the current of backward route is higher than the forward one, which is an evidence showing NC-effect on I_dV_{gs} of nFinFET.

B. Effects of Annealing Temperatures on HZO MIM

We show C_{NC} of HZO-gated nFinFET at different annealing temperatures(T) of HZO (Fig.5). Fig. 6 is the result of Fig. 5. Under the condition at V_{gs}-V_t=0.8V, as T< 550^{0}C, C_{NC} is positive, but it turns to be negative as T> 550^{0}C, which means NC effects just happen when T > 550^{0}C. However, after 550^{0}C, C_{NC} decays inversely. On the other hand, in Fig. 7, hysteresis (V_{hys}) is the largest as T<550^{0}C and maintains a relatively higher level at T= 550^{0}C ~600^{0}C but decays quickly while T>700^{0}C. To explain C_{NC} and V_{hys} obtained in Figs. 6 and 7, we divide T into 3 phases (Fig. 8). At phase I, T<550^{0}C, bulk traps(V^{2+}) dominate in HZO. V^{2+}-O^{2-} will induce dipole charges, in addition to few bulk dipoles, resulting in a significant V_{hys}. However, V^{2+}-O^{2-} cannot contribute to NC effect. Thus, C_{NC} is positive in phase I. As T rises to 600^{0}C, phase II, higher T passivates bulk traps and helps to generate more bulk dipoles, resulting in the occurrence of negative C_{NC}. Thanks to elimination of bulk traps, V_{hys} starts to decrease. When T > 600^{0}C (phase III), the amorphous state of HZO changes into polycrystalline and grains form. Leakage current flows easily through boundaries, and C_{NC} and hysteresis drops at T= 700^{0}C.

C. Short-channel Effect of NC-FinFET

Fig. 9 shows I_dV_{gs} of HZO-gated nFinFET. σV_t of the backward route is much smaller than that of forward one since a dipole built-in field of HZO enhances gate controllability of nFinFET. Moreover, DIBL of backward route decays with increasing V_{ds}, which is a typical NC effect. (Fig. 10) SS of back-branch I_dV_{gs} also improves owing to NC effect, but SS slowly increases along with V_{ds} because a higher V_{ds} reduces the gate coupling of HZO so as to decay the NC effect (Fig. 12). Then, in Fig. 9, I_{off} of the backward route is clearly larger than that of the forward one because the dipole built-in field of HZO increases gate leakage (Fig.13). As a result, NC effects strengthen short-channel effect not only in a smaller SS but also a better σV_t and a negative DIBL effect. However, I_{off} increases as a drawback.

D. Body Effect of NC-FinFET

By applying a larger V_{bs}, we can observe a shift of V_t which is a classical body effect (Fig. 14). Fig. 15 shows V_t trend of forward and backward routes as function of V_{bs}. Compared to that of forward route, V_t increase of backward route is more sensitive to V_{bs}, resulting in a decrease of hysteresis, which even approaches zero. In addition to the extraction of negative C_{NC}, we developed another approach to obtain C_{NC} by body sensitivity ($\delta V_t/\delta V_{bs}=C_{dm}/C_{ox}$). The results have shown that C_{NC} becomes more negative as V_{bs} boosts (Fig. 16). Furthermore, SS of the backward branch with the increase of V_{bs} is steeper than that of the forward one since a lower C_{dm} induced by body biases and a higher C_{ox} caused by NC effects (Fig. 17). Since hysteresis can be excluded by a suitable V_{bs}, by taking this benefit, a near hysteresis-free can be achieved, Fig. 18.

In summary, we have developed simple approaches to successfully characterizing negative capacitances in an HZO-gated FinFET. An appropriate annealing temperature (550^{0}C) is necessary to create NC effect inside HZO, which can be well explained by growth mechanisms of HZO. In terms of the short-channel effect, we clearly observed negative DIBL effect. Moreover, new findings include: σV_t is dramatically suppressed but I_{off} enlarges reversely as NC effect appears. Moreover, we can achieve a hysteresis-free NC-FET by applying a suitable V_{bs}. Furthermore, V_{bs} was also reduced S.S. Through these efforts, device physics of NC- FinFET can be well-understood, which will be helpful for design and fabrication of chips with ultra-low power and high performance in a near future.

Acknowledgments This work was support in part by the *Ministry of Science and Technology, Taiwan,* under *Research of Excellence program contract No. 107-2633-E009-003.*

References:[1] K. S. Li, et al., ***IEEE IEDM***, p. 620, 2015. [2] E. Ko, et al., ***IEEE EDL***, p. 418, 2017. [3] A. Rusu, et al., ***IEEE IEDM***, p. 395, 2010. [4] T. S. Böscke, et al., ***APL,*** p. 102903, 2011. [5] K. Mistry, et al., ***IEEE IEDM***, p. 247, 2007. [6] W. X. You, et al., ***IEEE TED***, p. 3476, 2017.

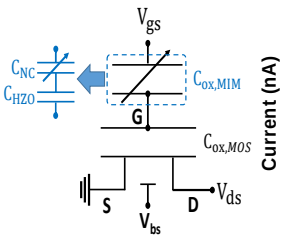

Fig. 1 The fabricated HZO-gated nFinFET in this study. $C_{ox,MIM}$ is molded as a series connection of C_{HZO} (ferroelectric cap.) and C_{NC}(NC cap.)

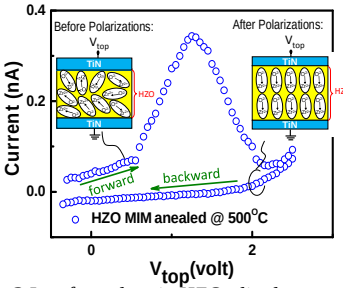

Fig. 2 In a ferroelectric HZO, dipoles are randomly distributed as V_{top} sweeps forward. However, the dipole field will be built and polarized when V_{top} sweeps backward. As a result, NC effect exists when polarized in the backward direction.

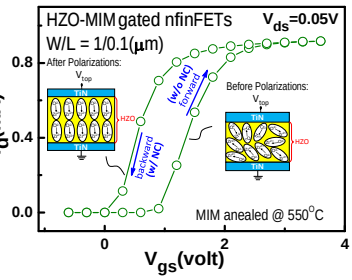

Fig. 3 The measured hysteresis of HZO-FinFET(**Fig. 1**). We can separate the forward and backward curves into I_dV_{gs} w/o NC effect(the forward) and I_dV_{gs} w/ NC effect(the backward).

$$\begin{cases} I_{d,f} = C_{ox,f}\mu_{eff}\frac{W}{L}(V_{gs}- V_{t,f} - \frac{1}{2}V_{ds})\,V_{ds}, & (1)\\ I_{d,b} = C_{ox,b}\mu_{eff}\frac{W}{L}(V_{gs}- V_{t,b} - \frac{1}{2}V_{ds})\,V_{ds}, & (2)\end{cases}$$

$$V_{hys.} = V_{th,f} - V_{th,b}. \qquad I_{d,f}: I_{d,forward},\ I_{d,b}: I_{d,backward} \quad (3)$$

$$\begin{cases} I_{d,f} = C_{ox,f}\mu_{eff}\frac{W}{L}(V_{gs}- V_{th,f} - \frac{1}{2}V_{ds})\,V_{ds}, & (4)\\ I'_{d,b}=C_{ox,b}\mu_{eff}\frac{W}{L}(V_{gs}- V_{th,b}- V_{hys.}- \frac{1}{2}V_{ds})\,V_{ds}, & (5)\end{cases}$$

$$\frac{(5)}{(4)} = \frac{I'_{d,b}}{I_{d,f}} = \frac{C_{ox,b}}{C_{ox,f}} \quad (6);\quad C_{ox,b} = \frac{I'_{d,b}}{I_{d,f}}C_{ox,f}. \quad (7)$$

$$C_{ox,b} = C_{ox,MOS} \parallel C_{ox,MIM} \quad (8);\ C_{ox,MIM}=C_{NC} \parallel C_{HZO} \quad (9)$$

$$C_{NC} = 1/(I_{d,f}/(I'_{d,b}C_{ox,f}) - 1/C_{ox,MOS} - 1/C_{ox,HZO}) \quad (10)$$

Table 1 The formulas to derive the NC values, in which Eq. (10) can be calculated from the measred forward, backward currents, and the NC effect and the respective ferroelectric and transistor capacitances.

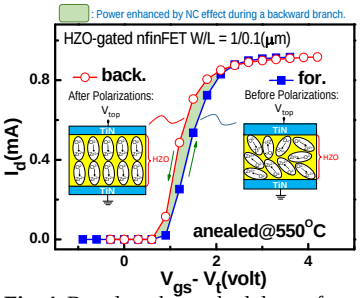

Fig. 4 Based on the methodology of **Table 1**, the difference between 2 curves is clearly observed, which is owing to NC-effect enhanced $C_{ox,b}$ of I_dV_{gs}.

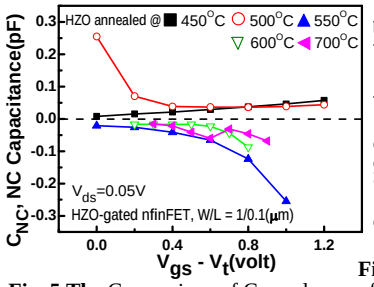

Fig. 5 The Comparison of C_{NC} values for HZO MIM with different annealing temperatures(T). The C_{NC} becomes negative as T > 500 ˚C. The strongest NC effect happens at T = 550 ˚C.

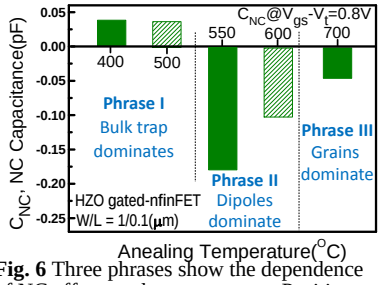

Fig. 6 Three phrases show the dependence of NC effect on the temperature. Positive C_{NC} in phase I is due to bulk traps. Polarized dipoles in HZO MIM result in significant negative C_{NC} in phase II. Reduced negative C_{NC} in phase III caused by leakage current through grain boundaries in HZO bulk.

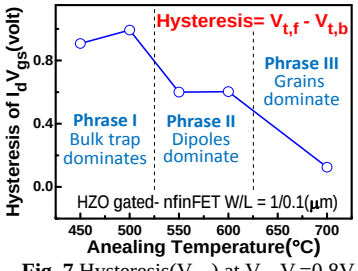

Fig. 7 Hysteresis(V_{hys}) at V_{gs}-V_t=0.8V. Significant V_{hys} in phase I is caused by bulk traps. AsT increases, traps are alleviated; dipoles generate, which remains V_{hys} in 550 & 600 ˚C. V_{hys} reduces in phase III because of leakage current through grain boundaries in HZO.

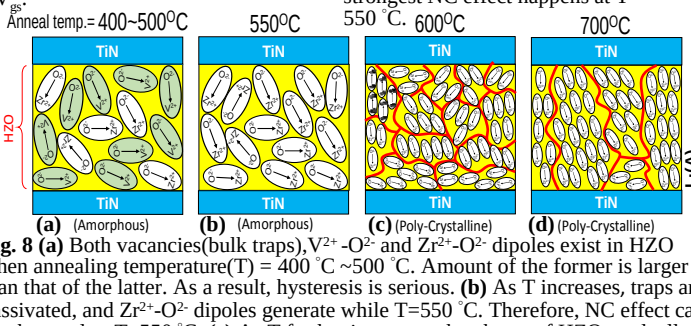

Fig. 8 (a) Both vacancies(bulk traps), V^{2+}-O^{2-} and Zr^{2+}-O^{2-} dipoles exist in HZO when annealing temperature(T) = 400 ˚C ~500 ˚C. Amount of the former is larger than that of the latter. As a result, hysteresis is serious. **(b)** As T increases, traps are passivated, and Zr^{2+}-O^{2-} dipoles generate while T=550 ˚C. Therefore, NC effect can be observed as T>550 ˚C. **(c)** As T further increases, the phrase of HZO gradually changes from amorphous to poly-crystalline; grains form in HZO as T approaches 600 ˚C. **(d)** Grains grow even larger when T reaches 700 ˚C. The leakage can flow through boundaries, in terms of reduction of both C_{NC} & V_{hys}.

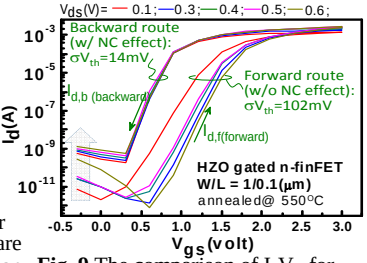

Fig. 9 The comparison of I_dV_{gs} for different V_{ds}. $I_{d,b}$ with NC effect exhibits a better σV_{th} than $I_{d,f}$ without NC, in terms of a better short channel effect. But I_{off} increases reversely when NC effect exists.

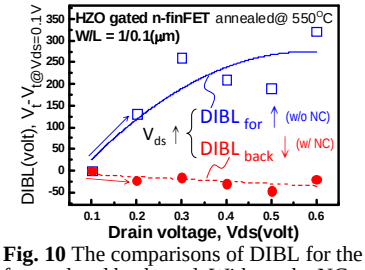

Fig. 10 The comparisons of DIBL for the forward and backward. Without the NC effect, the DIBL increases as V_{ds} raises; however, with NC effect, it decays inversely when V_{ds} increases.

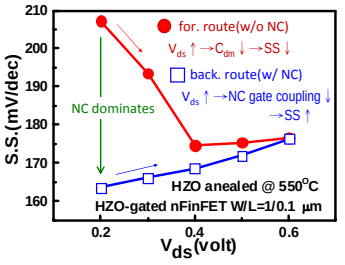

Fig. 11 Without NC, S.S. of the back-branch is steeper than that of the for-one w/o NC, but it slowly increases as V_{ds} ramps because the NC gate coupling effect is reduced when V_{ds} increases.

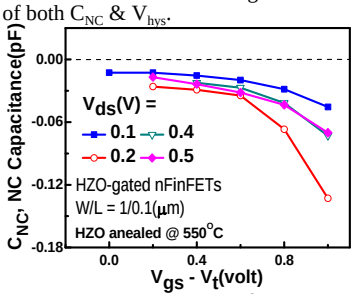

Fig. 12 The comparison of C_{NC} as function of V_{ds}, it is double confirmed that C_{NC} decreases when V_{ds} is raised because of the reduction for gate-coupling of C_{NC} to the channel.

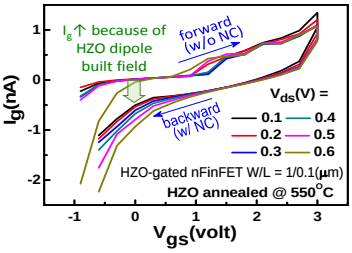

Fig. 13 In **Fig. 9**, it was observed that, w/ NC, the I_{off} increases, which can be well explained that the electric field built by dipoles inducing the gate leakage of nFinFET.

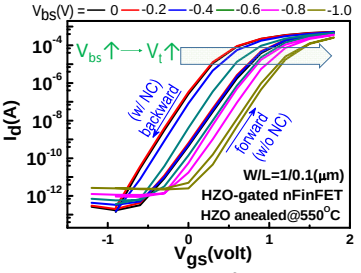

Fig. 14 The comparison of I_dV_{gs} w/o NC(forward) and w/ NC(backward) as function of V_{bs}. The typical body effect has been observed. The larger the V_{bs} is, the higher the V_t becomes.

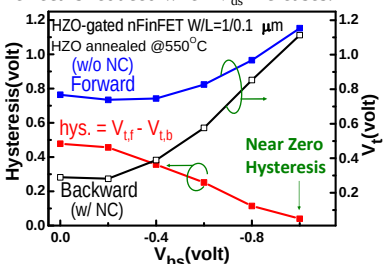

Fig. 15 Body sensitivity ($\delta V_t/\delta V_{bs}$) of the backward with NC is more sensitive than that of the forward without NC such that hysteresis reaches zero at a larger V_{bs}.

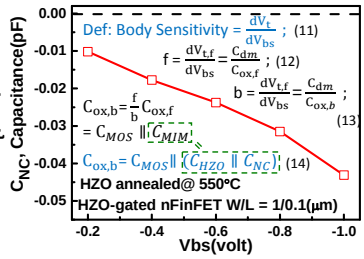

Fig. 16 Body sensitivity ($\delta V_t/\delta V_{bs}$)= C_{dm}/C_{ox}. We can directly extract C_{NC} as function of V_{bs} through the body sensitivity. C_{NC} increases as V_{bs} is raised.

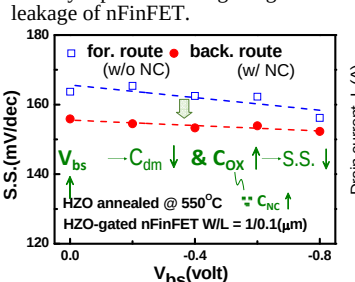

Fig. 17 The larger V_{bs} is, the smaller S.S. becomes, owing to reduced C_{dm} and increased C_{ox}. The former is a body effect; the latter is because C_{NC} enlarges as V_{bs} is raised.

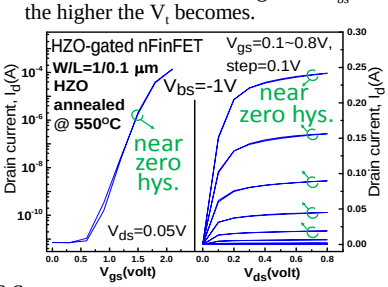

Fig. 18, The body bias can be applied to achieve a zero-hysteresis and a low Ioff leakage.