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# On the Physical Origin of Steep Subthreshold Slope in Ferroelectric FET: Transient Negative Capacitance Effect Caused by Polarization Switching Delay

Chengji Jin, Toshiro Hiramoto, and Masaharu Kobayashi

Institute of Industrial Science, The University of Tokyo, 4-6-1 Komaba, Meguro-ku, Tokyo 153-8508, Japan
Phone: +81-3-5452-6264 E-mail: cjjin@nano.iis.u-tokyo.ac.jp

**Abstract**

**We have investigated steep subthreshold slope (SS) phenomenon in ferroelectric FET by transistor level simulation based on time-delayed Preisach model calibrated by transient measurement of ferroelectric $HfO_2$, for the first time. Transient negative capacitance (NC) effect caused by polarization switching delay results in sub-60 mV/dec SS with practical material, device and measurement parameters. The model provides a reasonable interpretation to the previously reported steep SS in NCFET.**

## 1. Introduction

For future energy-efficient computing, Ferroelectric FET (FeFET) with sub-60mV/dec subthreshold slope (SS), which is also called negative capacitance FET (NCFET), has been proposed [1]. NC effect was originally proposed by the theory that the unstable negative slope region in S-shaped Polarization-Voltage (P-V) curve of ferroelectric (FE) can be stabilized and accessed with an appropriate positive capacitor connected in series [1, 2]. According to this theory, the capacitance matching for steep SS is achieved near inversion region instead of subthreshold region with standard channel design. However, many experimental results of long channel transistors show steep SS in deep subthreshold region with negligible hysteresis in quasi-static condition, which may not be fully explained only within the framework above [3-5]. Moreover, how such a stabilized state is established at microscopic level is elusive [6].

Recently, the classical Preisach model of FE, which is a macroscopic model taking into account multi-domain effect and dynamic behavior of FE, was revisited and well explain the transient NC effect observed in Resistor-Metal/FE/Metal (R-MFM) or Resistor-Metal/FE/Insulator/Semiconductor (R-MFIS) netlist as well as FE-dielectric (DE) series capacitor [6-9]. However, whether it can also explain the steep SS observed in transistor remains uncertain and needs to be investigated. In this paper, we demonstrate transistor level simulation of NC effect with time-delayed Preisach model and investigate sub-60mV/dec SS phenomenon.

## 2. Model Description and Simulation Method

Preisach model implemented in this simulation is described in Fig. 1. It consists of three parts: (1) quasi-static P-V curve of FE capacitor, (2) polarization switching delay caused by domain nucleation and domain-wall propagation, and (3) paraelectric component. Here $P_r$ is remnant polarization, $P_s$ is saturation polarization, $V_c$ is coercive voltage, $V_{fe}$ and $V_{aux}$ are voltage drop across FE component with and without delay, $\tau$ is polarization switching delay, and $\varepsilon_r$ is relative dielectric constant of paraelectric component [9-11]. All these equations are solved by combining with 2-D Poisson's equation and carrier continuity equation self-consistently.

## 3. Result and Discussion

**Model verification and parameter extraction**

To verify this model and extract parameters of FE, quasi-static free carrier charge (Q)-V curve of 10 nm FE is simulated and fitted to our previous experimental result of FE-$HfZrO_2$ (HZO) in Fig. 2 (a) [12, 13]. Meanwhile, the experimental displacement current of this MFM capacitor in response to a triangular waveform can be reproduced with the same fitting parameters (Fig. 2 (b)).

In order to extract $\tau$, R-MFM netlist which is the same as experimental set-up in Ref. [12] is reconstructed in simulation. Fig. 3 shows transient response of R-MFM netlist (bottom inset of Fig. 3) where R=20 kΩ and input voltage pulse is from -4 V to 4 V. For the best fitting, $\tau$=4 μs is obtained. Top inset of Fig. 3 shows extracted Q-$V_{fe}$ curves where transient NC effect is directly observed.

By using the FE parameters extracted above, FE-DE series capacitors in response to a triangular waveform (inset of Fig. 4) is simulated. Fig. 4 plots internal voltage amplification ($A_v$) as a function of gate voltage. $A_v$ larger than 1 is observed near zero gate voltage for $\tau$=4 μs. Fig. 5 shows Q-$V_{fe}$ relation for FE, and NC effect is confirmed for $\tau$=4 μs. Similar NC effect in FE-DE series capacitors was experimental demonstrated in Ref. [7].

**Origin of NC effect**

Fig. 6 and 7 show simulated polarization switching current through FE (dP/dt) and free carrier current through series connected resistor (dQ/dt) as a function of time for R-MFM netlist with $\tau$=4 μs and 0. There is a time period when, following the increase of dP/dt, dQ/dt increases but dP/dt becomes larger than dQ/dt, for $\tau$=4 μs (Fig. 6). This period is exactly when NC effect happens. Initially after pulse input, voltage across the FE capacitor increases by charging paraelectric component. When dP/dt increases and dP/dt > dQ/dt, in order to satisfy charge balance: $Q=\varepsilon_0\varepsilon_r E_{fe}+P$, $E_{fe}=V_{fe}/t_{fe}$ has to decrease. dQ/dt is also driven by the increase of dP/dt, leading to increased voltage drop across resistor, which is the voltage amplification due to transient NC effect. This mechanism is also confirmed in FE-DE series capacitor, as illustrated in Fig.8.

**Steep SS in FeFET by transient NC effect**

MFIS-FeFET and reference MOSFET are simulated in a dynamic mode with finite voltage sweep time. Table. 1 summarizes device parameters. The sweep voltage amplitude of gate voltage ($V_g$), $V_s$, is set to be more than the maximum applied voltage in Fig. 2. First, $V_g = -V_s$ is applied for 10 μs to initialize polarization state. Then, forward sweep from $-V_s$ to $V_s$ followed by reverse sweep from $V_s$ to $-V_s$ at rate of 1 V/μs is applied. Drain voltage ($V_d$) is nominally 50 mV. Fig. 9 and 10 plot simulated $I_d$-$V_g$ curve and point SS, respectively. Sub-60mV/dec SS is achieved only for FeFET on reverse sweep because NC region is accessible in transition from inversion to subthreshold rather than from accumulation to subthreshold because of the charge balance based on Fig. 5. This characteristic is similar to experimental result in Ref. [5], but hysteresis is large. The smaller hysteresis could be obtained in thinner FE with smaller $E_c$. Slow trap and detrap may also compensate hysteresis [14].

To show the importance of $\tau$ for NC effect in transistor, Fig. 11 and 12 show $I_d$-$V_g$ and point SS for FeFET with $\tau$= 0 and $\tau$=4 μs, respectively. No NC effect happens when $\tau$= 0 and memory operation was confirmed which indicates that NC effect does not occur only by non-linear dielectric constant. For $\tau$=4 μs, if sweep rate decreases, NC effect becomes weaker as shown in Fig. 13. This result does not match to quasi-static NC effect observed in experiment. However, $I_d$-$V_g$ can remain the same if we decrease sweep rate and increase $\tau$ by the same order of magnitude in our simulation (Fig. 14 and 15). The reduced off-state current in Fig. 14 is due to reduced displacement current at lower sweep rate. The reported $\tau$ for 10 nm Si:$HfO_2$ in FeFET is from μs to ms [15]. With large $\tau$, it is possible to achieve sub-60mV/dec SS even at nearly quasi-static condition.

## 4. Conclusion

Transient behavior of FeFET is simulated based on time-delayed Preisach model. The result shows NC effect and sub-60mV/dec SS which is caused by polarization switching delay. Also, quasi-static sub-60mV/dec SS in the previously reported experiments can be explained by this model, if $\tau$ is large enough.

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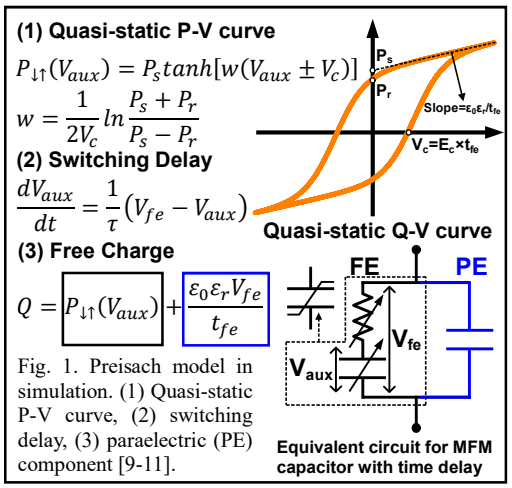


Fig. 1. Preisach model in simulation. (1) Quasi-static P-V curve, (2) switching delay, (3) paraelectric (PE) component [9-11].

| | $N_{sub}$ cm$^{-3}$ | $N_{S/D}$ cm$^{-3}$ | $T_{ox}$ nm | $T_{fe}$ nm | $L_G$ nm |
|---|---|---|---|---|---|
| **MOSFET** | P-type 6×10$^{17}$ | N-type 1×10$^{20}$ | 1 | - | 200 |
| **FeFET** | P-type 6×10$^{17}$ | N-type 1×10$^{20}$ | 1 | 5 | 200 |

Table. 1. Simulated device parameters

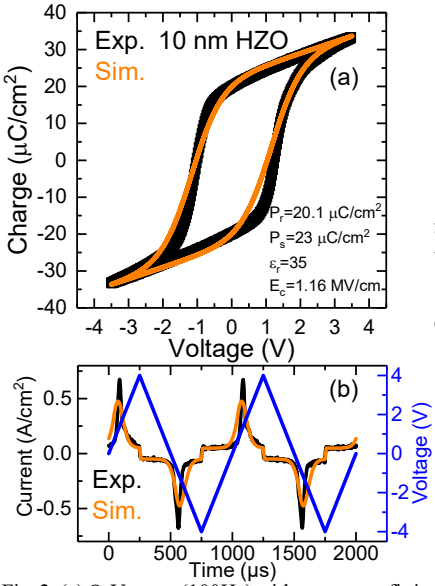


Fig. 2. (a) Q-V curve (100Hz) with parameter fitting for 10 nm HZO. (b) Displacement current of MFM capacitor in response to a triangular waveform with same parameter fitting [12].

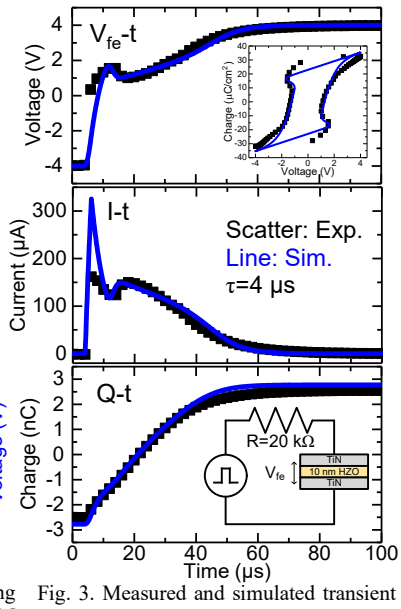


Fig. 3. Measured and simulated transient response of R-MFM. Top inset shows extracted Q-$V_{fe}$ curves. Bottom inset shows experiment and simulation set-up [12, 13].

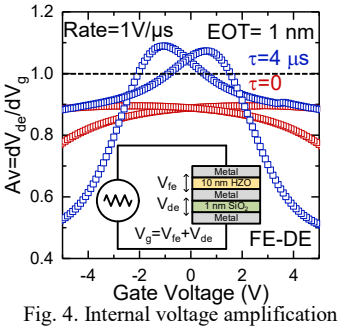


Fig. 4. Internal voltage amplification (Av) as a function of gate voltage.

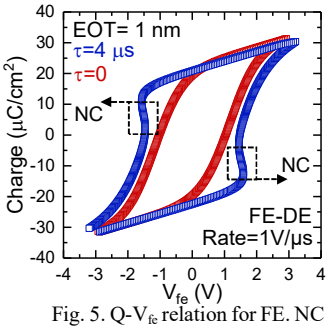


Fig. 5. Q-$V_{fe}$ relation for FE. NC effect is observed for τ=4 μs.

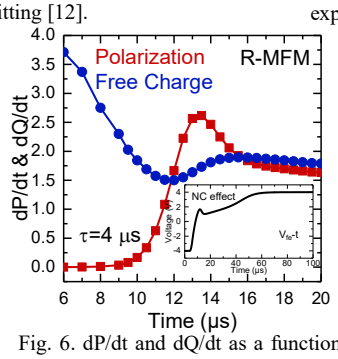


Fig. 6. dP/dt and dQ/dt as a function of time for R-MFM netlist with τ=4μs.

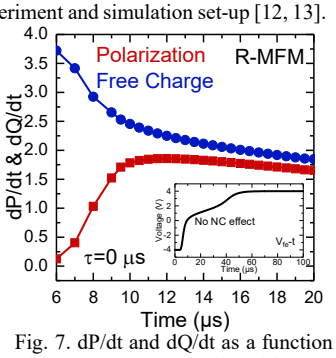


Fig. 7. dP/dt and dQ/dt as a function of time for R-MFM netlist with τ=0.

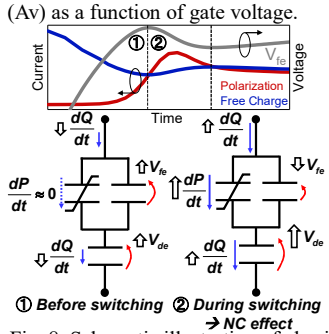


Fig. 8. Schematic illustration of physical mechanism of transient NC effect.

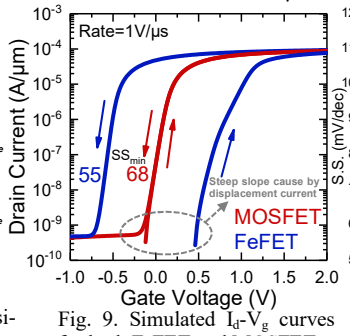


Fig. 9. Simulated $I_d$-$V_g$ curves for both FeFET and MOSFET.

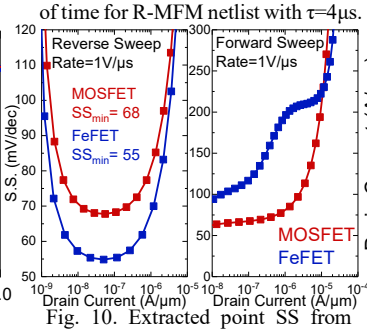


Fig. 10. Extracted point SS from Fig. 9. Sub-60 SS is achieved only for FeFET on reverse sweep.

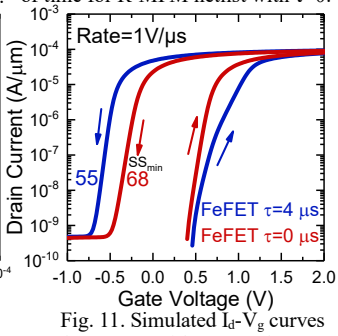


Fig. 11. Simulated $I_d$-$V_g$ curves for FeFET with τ= 0 and 4 μs.

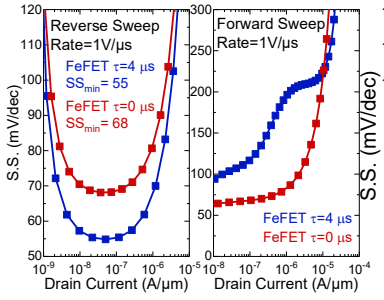


Fig. 12. Extracted point SS from Fig. 11. No NC effect happens when τ= 0.

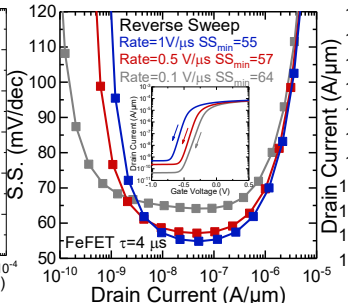


Fig. 13. SS for same τ=4 μs, different sweep rate. Inset shows $I_d$-$V_g$ curves.

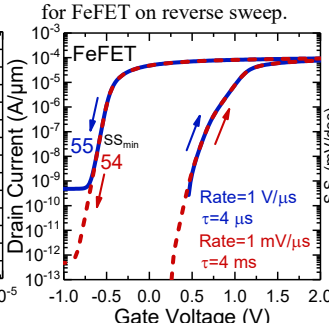


Fig. 14. Simulated $I_d$-$V_g$ with two different sets of sweep rate and τ.

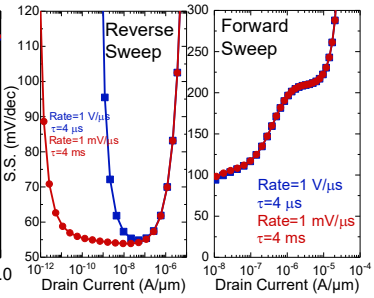


Fig. 15. Extracted point SS from Fig. 14.

**References**

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