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Investigation of Switching Characteristics for Silicon Doped Hafnium Oxide FeFET

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Abstract

We report insight on the performance of a gate first MFIS-HfO_2 FeFET memory using a SiO_2 interface layer. The FeFET devices show FE switching characterized by V_T distribution for program/erase states. The endurance and memory window characteristic shows the effect of interface layer permittivity and charge trapping on FeFET performance. A small read disturb and 10 years extrapolated retention were measured for the devices.

1. Introduction

The growing demand for NVMs especially into highly scaled nodes, renewed the interest into emerging memory concepts. Limited in scalability, interest into ferroelectric (FE) memories such as FeFETs was revived by the inception of ferroelectricity in high-k oxide HfO_2 [1]. Due to its high FE coercive field, FeFET scaling is achieved in an embedded integration scheme even to the smallest nodes [2]. A major advantage of FE memories such as FeFETs is their notably lower power and higher speed operation capability as compared to the mainstream Flash technology. Yet, the FeFET performance is strongly dependent on fabrication aspects of the integrated device and the effect of overall flow thermal budget on the FE film properties. In this paper, we report the integration of MFIS-HfO_2 FeFET in a gate first scheme. The FeFET performance with SiO_2 interface layers is discussed to give more insight on the potential performance capability of FE-HfO_2 based FeFET memory.

2. Device Fabrication

Initial 300 mm low B-doped wafers with 100 nm of thermally grown field oxide were used for the FeFET integration flow (Fig. 1). The FeFET active area was defined by etching field oxide in a two-step etching sequence. The SiO_2 interface layer (~ 1 nm) of the MFIS stack was wet chemically grown on the channel surface, which was followed by an ALD deposition of 10 nm silicon doped hafnium oxide (Si:HfO_2) using optimum Si content for the FE film. The top gate electrode consisted of a 10 nm PVD processed TiN metal layer and a 100 nm of phosphorus doped amorphous silicon (P:aSi). In a second lithography step, the gate area is defined (Fig. 2) whereas the gate stack is subsequently etched beginning with 100 nm of P:aSi (RIE etching) as well as TiN (SC1) and eventually by etching 10 nm HfO_2 (RIE etching) to the substrate surface. The phosphorus dopant ion implantation to form the S/D junctions was done with a 10 nm ALD processed SiO_2 scatter layer. The gate stack side walls were covered using SiO_2 spacers that were etched after the S/D dopant activation anneal.

3. Results and Discussion

The FeFET memory exhibits characteristics as in Fig.3a where the V_T shift of the transistor is controlled by the FE polarization switching. Thus, the V_T shift depends on the applied field across the FE material/gate stack (Fig. 3b, c). The difference between V_T for program (PG) and erase (ER) defines a memory window (MW) trend (Fig. 3d) as measured using symmetric pulse amplitude. This trend illustrates different FeFET operation modes ranging from non-switching, FE switching to trap dominated operation where the FE dominated channel control is compensated by trap charges in the Si:HfO_2 layer. However, for optimal switching condition, the V_T shift becomes dependent on FE domain orientations and its alignment with the field which in turn give rise to a PG/ER V_T distribution (Fig. 4a) and a MW probability distribution (Fig. 4b) as statistically measured over 500 devices of the same flavor on full wafer map. This in part is intrinsic to the polycrystalline FE film but also depending on the deposition process uniformity (Fig. 4c) as visible in a diagonal MW pattern over the wafer due to e.g. Si incorporation. A proper readout voltage can result in large I_{on}-I_{off} current ratios (Fig. 4d). The endurance characteristic in Fig. 5a is strongly dependent on the interface layer with SiO_2 revealing a symmetric FeFET V_T degradation of both states and thus MW closure (Fig. 5b). A parallel shift in the I_d-V_g curves (Fig. 5c) up to 10^4 cycles due to charge trapping in the gate stack whereas a slope degradation (Fig. 5d) dominated by interface trap generation [3] is observed for higher cycling ranges. The FeFET MW characteristics at low (Fig. 6a) and high (Fig. 6b) PG/ER amplitude indicates the transition from FE switching to a trap dominated regime. This trend depends on the interface layer and its relative permittivity to the FE layer. Due to the low permittivity of SiO_2, a higher voltage drop occurs at the interface leading to improved tunneling that feature time and amplitude dependent trend accompanied with trapping in the Si:HfO_2 and FE MW closure. The readout disturb is weak (Fig. 7a) and a 10 year data retention is extrapolated at RT (Fig. 7b) gives promising indications for FeFET as an NVM.

4. Conclusion

We reported insight on performance capability of MFIS-HfO_2 FeFET memory by illustrating characteristic trends of FE switching, statistical performance, endurance, and retention for a gate first integration using SiO_2 interface.

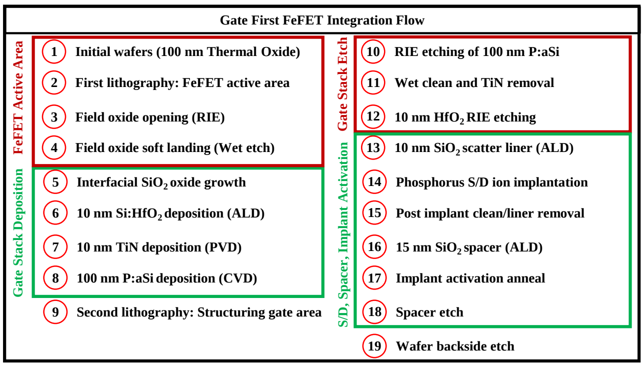

Fig.1 The integration flow of the FeFET devices illustrating the process steps based on gate first scheme.

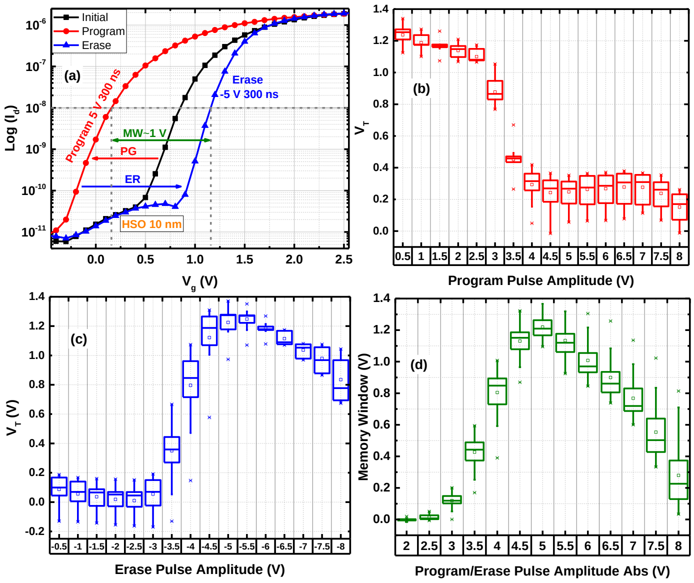

Fig.3 The FeFET Characteristics at 300 ns pulse width: (a) I_d-V_g corresponding to different FE material state, (b) PG V_T trend, (c) ER V_T trend, (d) FeFET MW using symmetric PG/ER pulses.

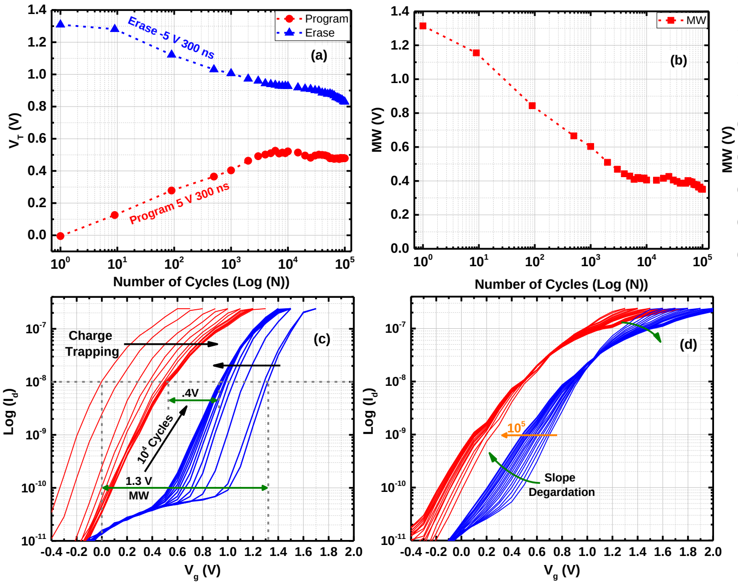

Fig.5 The FeFET endurance: (a) PG/ER V_T over cycling, (b) The MW variation over cycling, (c) I_d-V_g characteristics to 10^4 cycles, (d) I_d-V_g curves beyond 10^4 to 10^5 cycles.

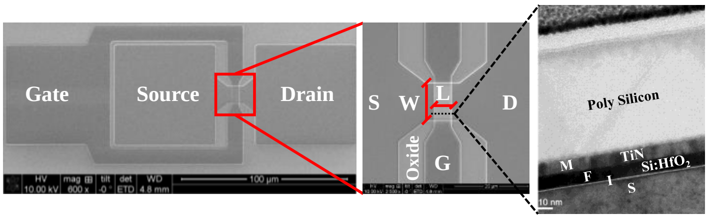

Fig.2 An SEM top view with TEM cross section of the FeFET devices.

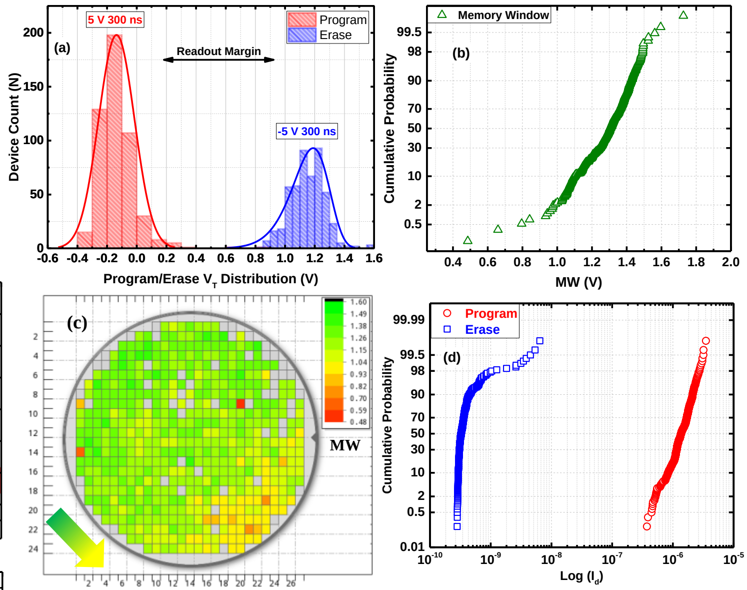

Fig.4 FeFET statistical trends: (a) V_T distribution for PG/ER states, (b) MW cumulative probability, (c) Full wafer map MW distribution, (d) I_{on}-I_{off} cumulative current probability distribution at .5V readout.

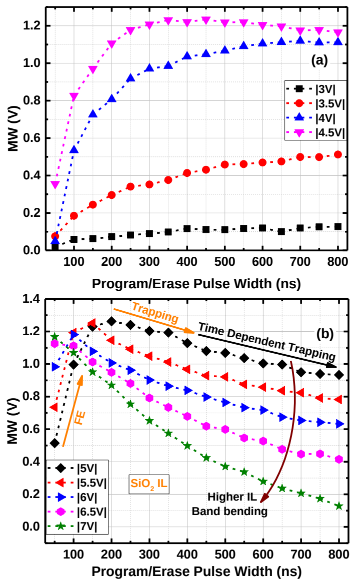

Fig.6 The FeFET MW trend dominated by: (a) FE switching, (b) Charge trapping

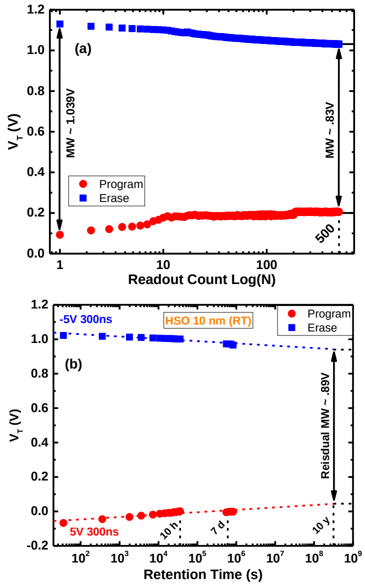

Fig.7 (a) FeFET readout disturb, (b) FeFET retention extrapolated for 10 years at RT.

Acknowledgements

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References

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