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Deep Experimental Analysis of Negative Capacitance in $HfZrO_x$-Based Field-Effect Transistors

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Abstract

We demonstrate negative capacitance (NC) effect in $HfZrO_2$ (HZO) based FETs. It is observed that the improved SS, I_{DS}, and G_m in HZO transistors over control devices always come with the internal voltage amplification (dV_{int}/dV_{GS} > 1), and the V_{GS} values of that correspond to the negative slope of polarization switch, i.e. NC of HZO. The stable negative C_{FE} with its magnitude larger than the underlying C_{MOS} contributes to the non-hysteretic characteristics in the NC transistor.

1. Introduction

Negative capacitance (NC) FET is a promising candidate for ultra low power applications, due to its sub-60 mV/decade subthreshold swing (SS) by ferroelectric (FE) [1]-[3]. Many works have been reported the demonstration of NC in FE capacitor and NC FETs [4]-[6]. NC was inverstigated by measuring the voltage drop across FE V_{FE} with voltage sweeping by a time-resovled measurement [5]. Negative slope of polarization P versus V_{FE} curves indicating NC, has been observed in PVDF [4], $BiFeO_3$ [6], and PZT [7] transistors, however, all of which exhibited hysteresis.

In this work, we experimentally demonstrate NC in $HfZrO_2$ (HZO) FETs with hysteresis-free characteristics. Both steep SS and internal voltage gain (dV_{int}/dV_{GS} > 1) are dependent on negative slope P-V_{FE} in HZO.

2. Performance Improvement in NC transistors

Fig. 1 shows the schematic of the NC Ge pFET integrated with 4.5 nm HZO and control MOSFET. The fabrication process was described in [8]. Fig. 2(a) shows the measured I_{DS}-V_{GS} of a pair of NC Ge pFET and control device with a gate length L_G of 3.5 μm. NC transistor achieves the improved I_{DS} compared to the control device. Point SS versus I_{DS} curves in Fig. 2(b) show that the NC transistor has the improved SS over control. Fig. 2(c) shows that NC transistor obtains the significantly improved transconductance G_m over the control device. The statistical plots in Fig. 3 show that NC pFETs achieve 35.6%, 51.3%, and 63.5% performance improvement in I_{DS}, G_m, and average SS, respectively, compared to the control devices.

3. Polarization Switch in Ferroelectric

During the sweeping of V_{GS}, V_{int} can be extracted in NC transistor based on the fact that I_{DS}-V_{int} curve of NC transistor is exactly the same as the I_{DS}-V_{GS} curve of the control device. We, thus, plot the extracted V_{int}-V_{GS} and dV_{int}/dV_{GS} curves for NC device in Fig. 4(a) and (b), respectively. dV_{int}/dV_{GS} > 1 is obtained at a wide range of V_{GS}, leading to

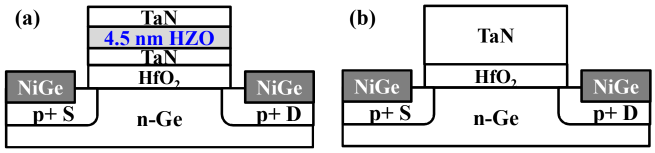

Fig. 1. Schematics of the fabricated NC Ge pFET integrated with 4.5 nm HZO and control MOSFET.

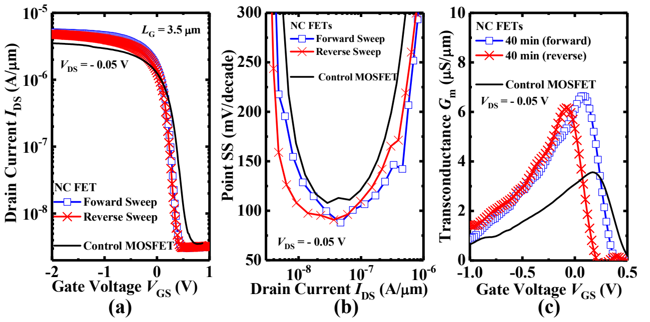

Fig. 2. (a) Measured I_{DS}-V_{GS} curves for a typical NC Ge pFET and control device. (b) Point SS versus I_{DS} characteristics of the same pair of devices. (c) G_m as a function of V_{GS} curves of the devices.

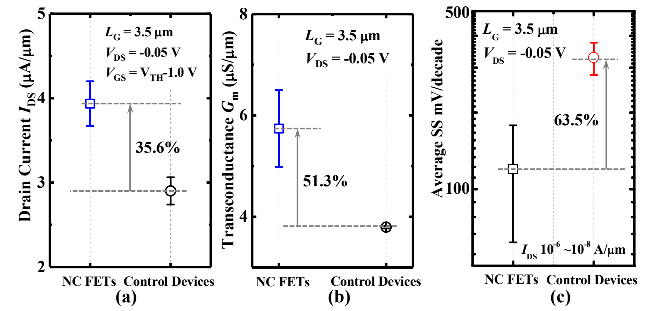

Fig. 3. Statistical plots of (a) I_{DS}, (b) G_m, and (c) average SS showing the improved electrical performance in NC Ge pFETs compared to control MOSFETs.

the steeper SS over control device in the whole measuring range of I_{DS}.

In NC transistors, the steep SS and hysteresis characteristics are dependent on the P switching in FE film. During the sweeping of V_{GS}, P of HZO is approximately equal to the charge density in channel region [9], due to the equal charge stored in C_{FE} and C_{MOS}, which can be achieved from capacitance curve integral. Fig. 5(a) shows the extracted C_{MOS} as a function of V_{GS} curves for NC transistor, based on the V_{int}-V_{GS} in Fig. 4(a) and the measured C_G-V_{GS} curves of control device. Accordingly, the P-V_{GS} curves of the device are obtained and shown in Fig. 5(b).

To get a deep insight into the NC in transistors, P-V_{FE} curves of HZO of the devices are plotted in Fig. 6(a). Loadlines, which was introduced in [10], are represented for the relation between distribution of V_{GS} and stored charge of underlying C_{MOS}. As shown in Fig. 6(a), the intersection of

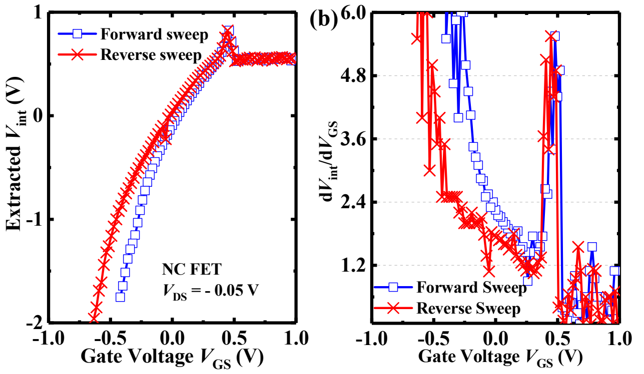

Fig. 4. Extracted (a)V_{int} and (b) dV_{int}/dV_{GS} versus V_{GS} characteristics for the NC Ge pFET.

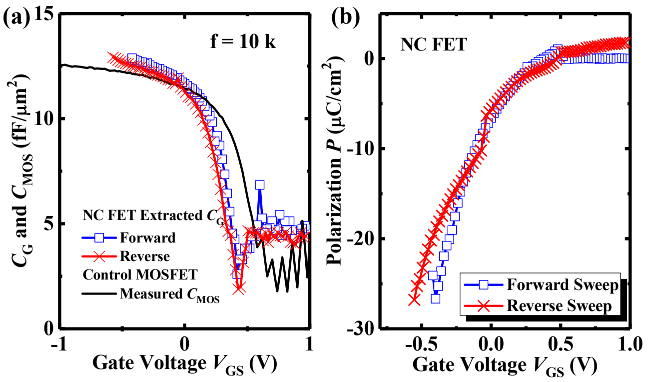

Fig. 5. (a) Extracted C_{MOS}-V_{GS} and measured C_G-V_{GS} curves of control device for NC transistor. (b) P-V_{GS} curves for the NC pFET with forward and reverse sweeping.

loadlines and P-V_{FE} curves decides the biasing voltages for C_{FE} and C_{MOS} [1], [3], [11]-[13]. Both forward and reverse sweeping demonstrate a wide negative slope region at V_{GS} -0.5 ~ 0.5 V, which contributes to the steeper SS of NC transistor compared to the control device. It is observed that the NC region, especially for the subthreshold region (0 V < V_{GS} < 0.4 V) has the much smaller P and the lower negative maximum V_{FE} values compared to the measured remnant P and coercive field, respectively, of HZO [14], [15]. It is speculated that the working mechanism of NC is not the switching of complete domain, but the domain wall.

We further compare the extracted C_{FE} i.e. dP/dV_{FE}, and C_{MOS} values in NC Ge pFETs in Fig. 6. From onset of NC, the magnitude of negative C_{FE} in transistor is always larger than C_{MOS} whatever forward or reverse V_{GS} sweeping [Fig. 6(b)]. The stable polarization switching is responsible for the non-hysteretic characteristics. In addition, the large internal gate gain dV_{int}/dV_G > 1 results from the small difference between $|C_{FE}|$ and C_{MOS} in the subthreshold region contributing to the steeper SS over the control transistor.

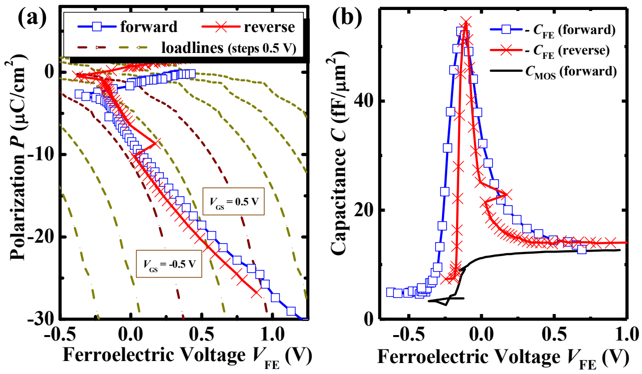

Fig. 6. (a) P-V_{FE} curves of NC Ge pFET with forward and reverse sweeping. (b) Comparison of C_{FE} and underlying C_{MOS} for the device.

3. Conclusions

We report the experimental study of negative slope of P-V_{FE} curves, *i.e.* NC effect in HZO FETs. For non-hysteretic NC transistors, the steep SS and dV_{int}/dV_{GS} > 1 occur at V_{GS}, where NC effective is observed. This demonstrates that the NC of HZO boosts the variation rate of V_{int}. During V_{GS} sweeping, the stable $-C_{FE}$>C_{MOS} effect observed contributes to the non-hysteretic characteristics in device. The different NC behaviors are considered to be related to the microscopic domain wall switching in FE thin films.

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References

[1] S. Salahuddin *et al.*, Nano Lett. 8(2008) 405.
[2] J. Zhou *et al.*, *IEEE International Electron Devices Meeting* (2016) 395.
[3] Z. Krivokapic *et al.*, *IEEE International Electron Devices Meeting* (2017) 357.
[4] A. Rusu *et al.*, *IEEE International Electron Devices Meeting* (2010) 395.
[5] P. Sharma *et al.*, IEEE Electron Device Lett. 39 (2018) 272.
[6] A. Khan *et al.*, IEEE Electron Device Lett. 37(2016) 111.
[7] A. Saeidi *et al.*, *ESSDERC* (2017) 78.
[8] Jing Li *et al.*, IEEE Electron Device Lett. 38 (2017) 1500.
[9] J. P. Duarte *et al.*, *IEEE International Electron Devices Meeting* (2016) 754.
[10] A. Khan *et al.*, IEEE Trans. Electron Device 63(2016) 4416.
[11] J. Jo *et al.*, IEEE Electron Device Lett. 37 (2016) 245.
[12] A. Khan *et al.*, IEEE Electron Device Lett. 38 (2017) 1335.
[13] G. Pahwa *et al.*, IEEE Trans. Electron Device 63(2016) 4981.
[14] J. Zhou *et al.*, *IEEE International Electron Devices Meeting* (2017) 373.
[15] G. Pahwa *et al.*, IEEE Trans. Electron Devic. 63 (2016) 4986.