Extended Abstracts of the 2018 International Conference on Solid State Devices and Materials, Tokyo, 2018, pp211-212

First Demonstration of Ferroelectric Lanthanum-Doped Hafnium Oxide for InGaAs Negative Capacitance MOSFET with Sub-60 mV/dec Subthreshold Swing

Quang-Ho Luc[1,2], Kai Yun Zhang[3], Chien Chou Fan-Chiang[4], Yu Da Jin[5], Huy Binh Do[1], Minh Thien Huu Ha[1], Sa Hoang Huynh[1], Ping Huang[2], Che-Wei Hsu[1], Sheng-Ping Wang[1], Yueh-Chin Lin[1], Edward Yi Chang[1,2,3*]

[1] Department of Materials Science and Engineering
[2] International College of Semiconductor Technology
[3] Department of Electronics Engineering
[4] Institute of Photonic System
[5] Institute of Lighting and Energy Photonics
National Chiao Tung Univ.
1001 University Road, Hsinchu 300, Taiwan
Phone: +886-3-5131502; E-mail: edc@mail.nctu.edu.tw

Abstract

In this work, we demonstrate ferroelectric (FE) La-doped HfO_2 (HLO) for the first time as a gate dielectric in order to realize InGaAs negative capacitance (NC) MOSFET. The steep subthreshold slope (*SS*) properties due to the NC effect are achieved at room temperature. The FE La:HfO_2 based $In_{0.53}Ga_{0.47}As$ NC MOSFET device exhibits counter-clockwise hysteresis in I_{DS}-V_{GS} characteristics as well as the minimal *SS* of 37 and 21 mV/dec for forward and reverse bias sweep, respectively.

1. Introduction

Ferroelectric (FE) materials with negative capacitance (NC) effects have been proposed to overcome the thermodynamic limitation of the subthreshold slope (*SS*) of 60 mV/dec for enabling next generation high operation performance and low power consumption CMOS devices [1]. NC field-effect transistors (FETs) have been introduced for Si and Ge-based devices with SS < 60 mV/dec [2]-[4]. InGaAs materials, owing to their extremely high electron mobility, are proposed as n-channel candidate to replace Si. Recently, the $In_{0.53}Ga_{0.47}As$ NC MOSFETs, using ferroelectric $HfZrO_2$ materials, has been reported with sub-60 mV/dec SS which is the first report for III-V-based nMOSFETs [5]. In this article, we fabricate and demonstrate InGaAs NC MOSFET by utilizing La-doped HfO_2 (HLO) thin film which has been proven to be one of the most promising FE materials. The NC characteristics are obtained only for HLO-based InGaAs MOSFET in comparison with other counterparts using Al_2O_3, HfO_2, and La_2O_3 gate dielectrics utilizing identical MOS interfacial passivation technique.

2. Experimental Procedure

The epitaxial structure used in this study consisted of 50 nm p-$In_{0.53}Ga_{0.47}As$ (5×10^{16} Be doped) channel layer and 100 nm p^+-InP buffer layer on the p^{++}-InP substrate grown by solid source molecular beam method. The gate-last process was used to fabricate the $In_{0.53}Ga_{0.47}As$ MOSFETs as described in Fig. 1. After surface degrease, 10 nm Al_2O_3 was grown by atomic layer deposition (ALD) as a dummy layer. Source/drain Si implantation was then performed and the dopant activation was carried out by rapid thermal annealing in a nitrogen ambient. The ALD precursors were TMA, TDMAH, La(^{i}PrCp)$_3$ and H_2O, and the ALD deposition temperature was 250 °C. After chemical pre-gate treatment with HCl and $(NH_4)_2S$, 10 half-cycles TMA pretreatment were performed in ALD chamber to further passivate the InGaAs surface [6] followed by 8 nm HLO deposition. Post deposition annealing (PDA) was performed at 500 °C for 5 minutes in forming gas. After TiN gate metal formation, post metallization annealing (PMA) was applied at 500 °C in N_2. Finally, Au/Ge/Ni/Au S/D ohmic, and AuBe backside contact were formed. Al_2O_3/InGaAs, HfO_2/InGaAs, and La_2O_3/InGaAs were fabricated by the same process flow and MOS interfacial passivation technique for comparison.

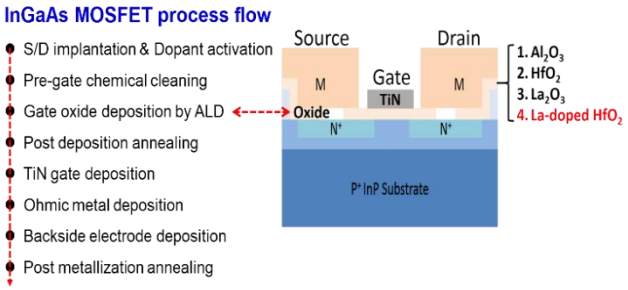

Fig. 1 Schematic diagram of device structure and gate-last process flow for the InGaAs MOSFETs.

3. Results and Discussion

Fig. 2 shows the transfer characteristics (I_{DS}-V_{GS}) of the (a) Al_2O_3/InGaAs, (b) HfO_2/InGaAs, (c) La_2O_3/InGaAs, and (d) HLO/InGaAs MOSFETs. All devices have a gate length of 6 μm and a gate width of 100 μm. The point *SS* characteristics of the fabricated InGaAs MOSFETs are presented in Fig. 3. The NC property can be clearly observed for the HLO/InGaAs MOSFET, resulting in the minimum *SS* of 37 and 41 mV/dec at V_{DS} of 0.05 and 1 V, respectively (Fig. 2(d)). This is attributed to the FE effect originated by the HLO thin film.

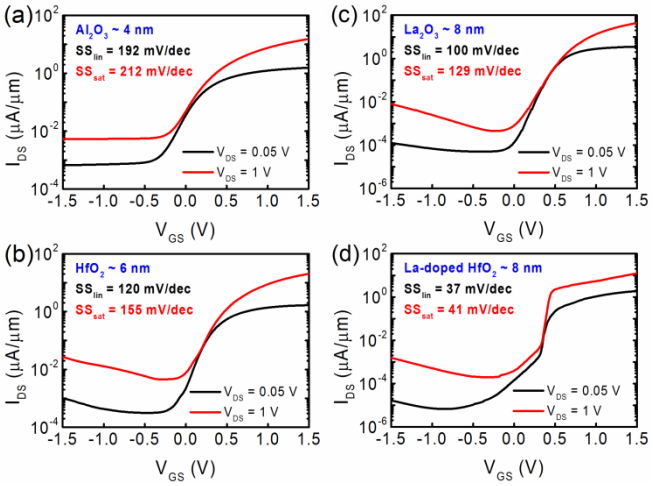

Fig. 2 The transfer characteristics (I_{DS}-V_{GS}) of the (a) Al_2O_3/InGaAs, (b) HfO_2/InGaAs, (c) La_2O_3/InGaAs, and (d) HLO/InGaAs MOSFETs. All MOSFET devices feature a gate length of 6 μm and a gate width of 100 μm.

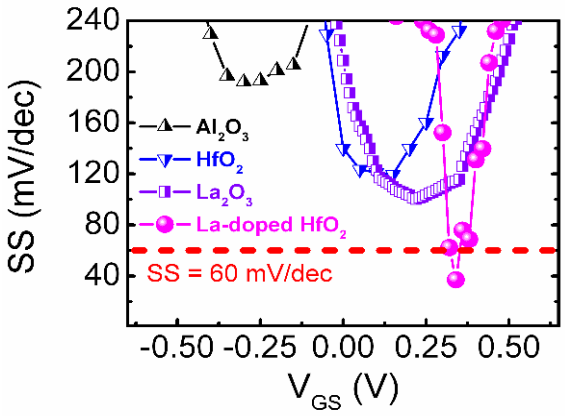

Fig. 3 The point *SS* characteristics against V_{GS} at V_{DS} of 0.05 V for the InGaAs MOSFETs with various gate dielectrics. The sub-60 mV/dec *SS* property can be observed only for FE HLO/InGaAs NC devices at V_{GS} of ~ 0.37 V.

The polarization-voltage (*P*-*V*) hysteresis of the HLO/InGaAs MOSCAPs is shown in Fig. 4(a). The ferroelectric hysteresis loops are obtained for HLO-based InGaAs MOS structure. The I_{DS}-V_{GS} at V_{DS} of 0.05 and 1 V, point *SS* follow I_{DS} and V_{GS} characteristics for the FE HLO/InGaAs NC MOSFET are shown in Fig. 4(b), (c), and (d), respectively. Very steep *SS* and counter-clockwise hysteresis in I_{DS}-V_{GS} characteristics can be clearly observed. This device exhibits the best point forward and reverses *SS* of 37 and 21 mV/dec, respectively, at a V_{DS} of 0.05 V accompanied with an I_{DS}-V_{GS} hysteresis of ~ 0.8 V. These results demonstrate that HLO/InGaAs MOSFET achieved in this work posses NC characteristics which can be attributed to the FE effects of the HLO material.

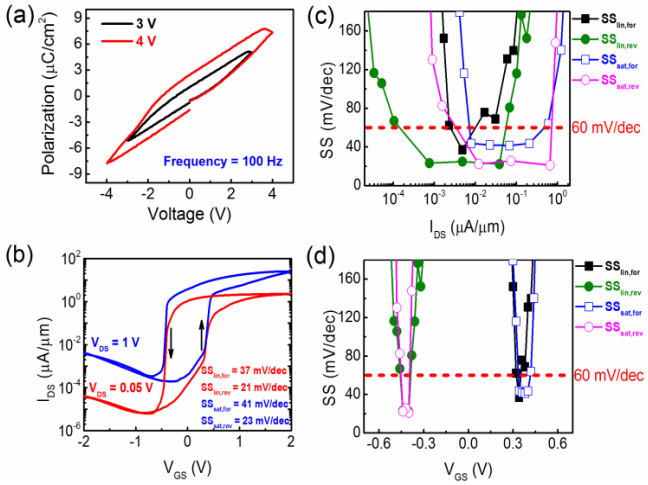

Fig. 4 (a) Polarization hysteresis loop of 8-nm HLO/InGaAs MOSCAP. The NC characteristics are originated from the FE effects. (b) Transfer characteristics (I_{DS}-V_{GS}) at V_{DS} of 0.05 and 1 V for the FE HLO/InGaAs NC MOSFET. The steeper reverse *SS* and I_{DS}-V_{GS} hysteresis of ~ 0.8 V are seen due to the capacitance non-match. This can be improved by adjusting the activation conditions and thickness of FE HLO materials system. The point *SS* characteristics against the (c) V_{GS} and (d) I_{DS} at V_{DS} of 0.05 and 1 V.

4. Conclusions

In summary, for the first time, we have proposed FE La-doped HfO_2 thin film in fabricating and demonstrating InGaAs negative capacitance MOSFETs. The minimal forward/reverse *SS* of 37 and 21 mV/dec are obtained. Steep *SS* characteristics due to the NC effect in HLO/InGaAs MOSFET device are achieved which is very promising for future ultra-low power consumption high speed III-V based logic applications.

Acknowledgements

This work was sponsored by the Ministry of Science and Technology, Taiwan, under Grant MOST 106-2221-E-009-142-MY2. The authors would like to thank to Dr. Jun-Fei Zheng and Dr. Tse-An Yeh from Entegris Inc. for their collaboration and support with the ALD precursors.

References

[1] S. Salahuddin *et al.,* Nano Lett. 8 (2008) 405.
[2] M. H. Lee *et al., International Electron Devices Meeting* (2015) 616.
[3] M. H. Lee *et al.,* IEEE Electron Device Lett.36 (2015) 294.
[4] J. Zhou *et al.,* International Electron Devices Meeting (2016) 310.
[5] Q.H. Luc *et al., Symposia on VLSI Technology and Circuits* (2018) T5-2.
[6] Q.H. Luc *et al.,* ECS Solid State Lett. 3 (2014) N27.