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# Mitigating edge effects in gate-normal tunneling field-effect transistors using a Ti/TiN dual-metal gate

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**Abstract**

**In this paper we discuss the implementation of a dual-metal gate in order to circumvent edge effects degrading the performance of gate-normal tunneling field-effect transistors. The use of two gate metals with different work functions, deposited by a self-aligned process, reduces the onset-voltage of gate-normal tunneling below that of adverse tunneling paths at edges. By this measure the steepest part of the current turn-on is restored, demonstrating how to experimentally eliminate a major issue related to this type of device geometry.**

## 1. Introduction

Tunneling field-effect transistors are actively studied because of their theoretical ability of obtaining subthreshold swings below 60 mV/dec, the thermal limit of MOSFETs at room temperature. Because of this, a reduced supply voltage $V_{dd}$ is sufficient for a full transition between the off- and on-state of a device. In turn, reduced $V_{dd}$ leads to reduced total power consumption, a perquisite for ultra-low power applications. However, achieving high performance like small SS and high $I_{on}$ in experiment is still challenging. A lot of effort is focused on understanding the origin of non-idealities e.g. to consequently avoid degradation from trap assisted tunneling [1]. In addition to that it has been pointed out that device geometries that rely on tunneling normal to the gate rather than lateral may exhibit steeper slopes and improved $I_{on}$. It was shown though, that this specific device architecture is prone to edge-effects which may severely degrade the device turn-on [2]. In this paper, we show experimentally how to improve device performances by using a dual-metal gate to suppress edge effects [3].

## 2. Experiments

*Device concept and Fabrication*

The devices are fabricated from a stack made of (from top to bottom) 40 nm n-Si, 100 nm i-Si, 30 nm i-$Si_{0.75}Ge_{0.25}$, 10 nm i-Si and 30 nm $p^+$-$Si_{0.5}Ge_{0.5}$ (Boron doping, $2x10^{20}$ $cm^{-3}$) grown by reduced pressure chemical vapor deposition on a 300mm Si(001) substrate. Using electron beam lithography and reactive ion etching, a pillar-shaped mesa is created by etching down the n-Si and i-Si layers and stopping when reaching the i-$Si_{0.75}Ge_{0.25}$ layer [Fig. 1(a)]. Subsequently, this i-SiGe layer is chemically removed using HF:$H_2O_2$:$CH_3COOH$ with a high selectivity to Si. The remaining i-Si layer on top of the $p^+$-$Si_{0.5}Ge_{0.5}$ layer surrounding the pillar form the gate-normal tunneling junction [Fig.2(a)]. Before gate-stack deposition, the i-Si layer thickness is reduced to about 5 nm by repeated cycles of oxidation and HF etching. 1 nm $Al_2O_3$ + 3 nm $HfO_2$ are deposited by atomic layer deposition as gate dielectric. The metal gate deposition composes a first optional step during which Ti is evaporated anisotropically onto the samples. Due to an undercut [Fig. 1(b)] at the bottom of the pillar, some regions are not covered because of shadowing effects. In the second mandatory step, atomic vapor deposition is used to conformally cover all parts of the pillar including the undercut with TiN. By this, two types of devices are realized: one with a single metal gate (TiN only) and another with a dual metal gate (Ti+TiN). The device processing is completed with $SiO_2$ passivation and the formation of TiN+Al contacts.

*Electrical characterization*

Fig. 2(a) shows the transfer characteristics of a device with a single metal gate (blue dashed lines). The drain-current $I_d$ slowly increases between 0.5 V < $V_g$ < 1.5 V. Above 1.5 V, $I_d$ increases with a steeper slope, which is still limited to about 250 mV/dec. [Fig. 2(b)]. By contrast, for samples that have

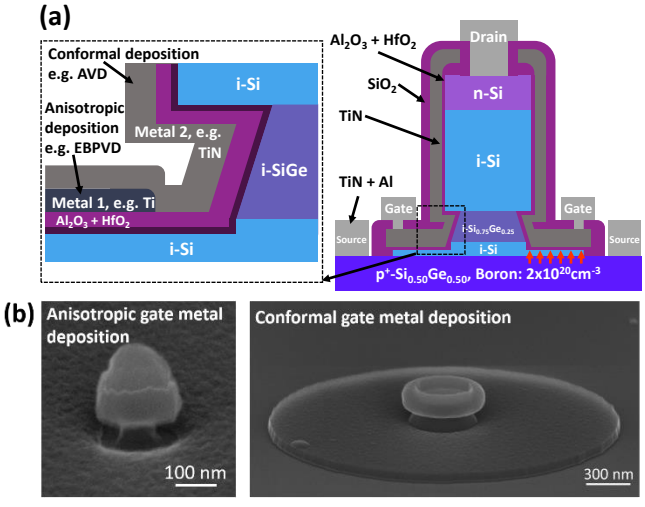


Fig. 1 (a) Device concept overview of a gate-normal TFET and zoom exemplifying the use of two gate metals. (b) SEM images illustrating the two-step self-aligned creation of a dual-metal gate utilizing anisotropic followed by conformal metal deposition.

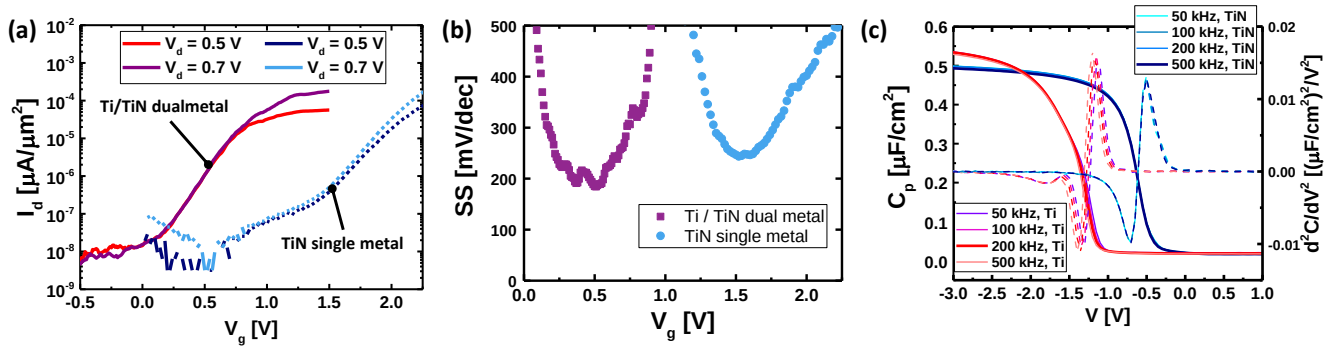


Fig. 2 (a) Transfer characteristics of devices with single (blue dashed lines) and dual-metal gates (red solid lines). The latter exhibits lower onset voltage and smaller $SS_{min}$ as evidenced in the SS vs. $V_g$ plot (b). (c) Determination of the work function difference $\Delta\Phi_m = \Delta V_{FB}$ with capacitance voltage measurements on Ti and TiN MOSCAPs.

been fabricated with a dual-metal gate, the divided turn-on is absent and a smaller SS down to 180 mV/dec is obtained. This improvement is related to a lower onset voltage which in turn stems from the smaller work function of Ti compared to TiN. The work function difference $\Delta\Phi_m$ is obtained from capacitance-voltage measurements on MOSCAPs as shown in Fig. 2(c). It is equivalent to the flat band voltage difference $\Delta V_{FB}$, for otherwise identical parameters, and is equal to 0.65 eV.

*Simulation and Interpretation*

The benefit of using a dual metal-gate can be clarified with the help of Sentaurus TCAD simulations employing a non-local band-to-band tunneling model and taking quantum confinement into consideration. The $I_d$-$V_g$ characteristics in Fig. 3(a) depict both cases of a single metal (brown line, $\Phi_{M1} = 4$ eV) and a dual-metal gate (light blue, $\Phi_{M1} = 3.6$ eV)

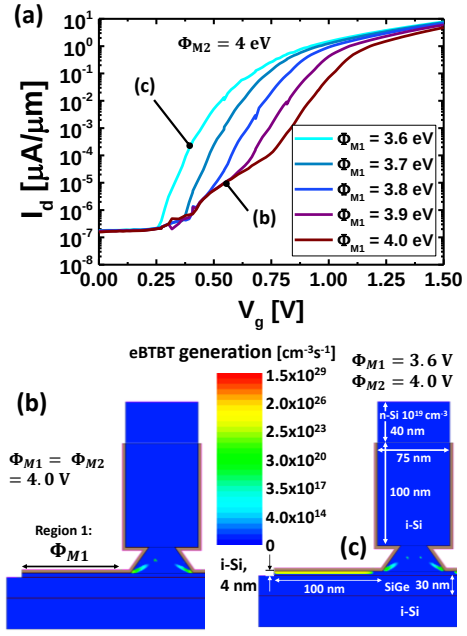


Fig. 3 (a) Simulated transfer characteristics emphasizing the necessity of using a dual metal gate to avoid a deteriorated subthreshold swing. In addition to a dual-metal gate, smaller EOT and thinner channel are required to boost the performance. (b) From eBTBT plots it becomes clear that premature tunneling into the pillar is the reason for the bipartite turn-on with a single gate-metal.

and reproduce the experimental traits [Fig. 2(a)] qualitatively. From the electron BTBT (eBTBT) generation plot in Fig. 3(b), it can be seen that the initial deficient increase of $I_d$ for a single metal gate originates from tunneling into the pillar from the source region directly below. By reducing the work function $\Phi_{M1}$ [Fig. 3(c)] the onset voltage of tunneling in region 1 is decreased below that of tunneling into the pillar. Thus, the complete turn-on is dominated by gate-normal tunneling, resulting in improved SS. Furthermore, the simulations show that tuning the onset of tunneling with different work functions is still important when the equivalent oxide thickness (EOT) and the Si channel thickness are small. At present, the ~1.5 nm EOT and a channel thickness of 5 nm limit the absolute performances. With a reduction of EOT to a state-of-the art value of 0.8 nm and a channel thickness of 4 nm, SS = 50 mV/dec and higher $I_{on}$ should become accessible using the proposed TFET geometry and the dual metal gate approach, as our simulations [Fig. 3(a)] suggest.

## 3. Conclusion

Our experiments have proven that in order to avoid a degraded SS stemming from parasitic tunneling at the edges of a gate-normal tunneling junction, a dual-metal gate can be employed. By mitigating edge effects, an unperturbed turn-on was achieved. As our simulations show, this is a perquisite for further improvements stemming from EOT and channel thickness scaling.


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