Demonstration of Ge Complementary Tunneling Field-Effect Transistors with Dopant Segregation NiGe Source/Drain

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Abstract
The Ge complementary tunneling field-effect transistors (TFETs) are fabricated with NiGe metal source/drain structure. The dopant segregation technique is employed to form the NiGe/Ge tunneling junctions with sufficiently high Schottky barrier heights. As a result, the Ge p- and n-TFETs exhibit decent electrical properties of on-state current and sub-threshold slope.

1. Introduction
Tunneling field-effect transistors (TFETs) have been investigated extensively as they promise the sub-threshold swing (S factor) of sub-60 mV/dec at room temperature, a key to reduce the power consumption in digital electronics [1-2]. However, on-state current (I\text{on}) in Si TFETs is well below that of MOSFETs. To achieve reasonable I\text{on} in TFETs, new channel materials with narrow band gap (E\text{g}) and small carrier effective mass are desired, such as Ge [3]. Unfortunately, it is extremely difficult to fabricate Ge source/drain (S/D) junctions with steep doping profiles by using the conventional ion implantation [4]. Thus, the NiGe Schottky junction is a promising S/D structure for Ge TFET since its abrupt NiGe/Ge metallic interface. Nevertheless, the Fermi level pinning effect at the NiGe/Ge interface makes it difficult to obtain a sufficiently large Schottky barrier height (SBH) for tunneling [5]. This phenomenon limits the performance enhancement of Ge TFETs. In this study, the Ge complementary TFETs were fabricated with the dopant segregation (DS) NiGe S/D structures. Due to the SBH modulations achieved by boron or phosphorous doping in the NiGe tunneling junctions (Fig. 1), the Ge p- and n-TFETs have been realized with I\text{on} of ~0.2 μA/μm at V\text{g}=V\text{d}=±0.5 V. Especially, a minimum S factor of 28 mV/dec at 7 K is revealed for Ge pTFETs.

2. NiGe/Ge Junctions with Dopant Segregation
The DS NiGe junctions were fabricated with gated guard ring structures (Fig. 2). After the pre-cleaning of Ge substrates (1016 cm\textsuperscript{-2}) and active area definition, the DS NiGe junctions were achieved by ion implantation, Ni deposition and rapid thermal annealing (RTA) in sequence. The MOS-structured guard ring was then formed by depositing Ni/Al\textsubscript{2}O\textsubscript{3} layers with ALD and thermal evaporation. Finally, the Ni and Al were deposited as contact pads. Fig. 3 shows the electrical properties of these DS modulated Schottky junctions. It is found that the Schottky junctions with sufficiently high SBHs can be achieved by using phosphorous DS (P-DS) and boron DS (B-DS). In order to further validate the DS method for TFET S/D fabrication, the rectifying characteristics of P-DS NiGe/n-Ge Schottky junctions were examined at 7 K with different guard ring voltage (V\text{r}). When the V\text{r} is decreased from 2 to -6 V, the DS NiGe/n-Ge Schottky junction is converted into a tunneling junction, along with the appearance of negative resistance in the forward junction voltage (V\text{f}) (Fig. 4). This phenomenon indicates a feasibility of the DS NiGe metallic S/D structure in Ge TFET technology.

3. Ge TFETs with the Dopant Segregation NiGe S/D
The fabrication process and device structures of the Ge p- and n-TFETs are shown in Fig. 5. Followed by active area definition, the DS NiGe S/D structure were fabricated. The Ni/Al\textsubscript{2}O\textsubscript{3}/GeO\textsubscript{2} gate stack was then formed [7] and finally the Ni contact pads were deposited. The smooth MOS interface and a ~20-nm-thick NiGe junction are confirmed for the Ge TFETs (Fig. 6). Fig. 7 shows the I\text{d}-V\text{g} characteristics of the Ge p- and n-TFETs, and the normal operations were validated for the devices. The temperature dependence of I\text{d} is compared between pTFETs and nMOSFETs at a high normal field of V\text{g}=±5 V (Fig. 8). It is found that the I\text{d} increases for Ge p TFETs with an increase of temperature, while the I\text{d} of Ge pMOSFETs decreases with increasing the temperature due to the mobility degradation. This result justifies the existence of band-to-band-tunneling currents for the DS NiGe S/D TFETs. Fig. 9 further confirms the TFET operations for these devices that the I\text{d} of Ge TFETs is independent of the channel length, because the total resistance is dominant by the NiGe/Ge tunnel junction. The impact of equivalent oxide thickness (EOT) scaling is also examined by reducing the gate insulator thickness. Fig. 10 shows that the S factor decreases and the I\text{on} increases with a thinner EOT, suggesting that EOT scaling is beneficial for the performance enhancement of Ge TFETs. The low temperature measurements on I\text{d}-V\text{g} characterization for the Ge p- and n-TFETs were conducted. Fig. 11 shows the I\text{d}-V\text{g} curves of a Ge pTFET at different temperatures. It is found that the S factor is significantly decreased at a lower temperature, attributable to the frozen of interface traps distributed over the band gap. These interface traps may induce an increase to the trap-assisted-tunneling (TAT) current and severely degrade the S factors [8]. On the other hand, the I\text{on} is also suppressed apparently at lower temperatures, which is possibly caused by the increase of E\text{g} in Ge. The S factors extracted from the I\text{d}-V\text{g} characteristics of pMOSFET, p- and n-TFETs are summarized in Fig. 12 as a function of temperature. The pTFET with the S factors of 28 and 35 mV/dec have been revealed at 7 and 50 K, respectively.

4. Conclusions
In this study, the Ge complementary TFETs have been demonstrated using DS NiGe metal S/D structures. The Ge p- and n-TFETs exhibit the I\text{on} of ~0.2 μA/μm at V\text{g}=V\text{d}=±0.5 V. The S factor of 28 mV/dec at 7 K is revealed for Ge pTFETs. These results strongly indicate that the DS NiGe metal S/D is a promising structure for realizing Ge TFETs with decent electrical properties.

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References
1. Ion implantation S/D: Dopant diffusion

Dopant diffusion into the semiconductor.

2. Metal S/D: Atomic sharp interface

Atomic sharp interface at the metal and semiconductor interface.

Fig. 1. The Band diagram of ion implantation junctions and DS modulated metal/Ge Schottky junctions.

Pre-cleaning of Ge
Field oxide (SiO₂)
Active area etching
Ion implantation
Ni deposition and RTA (NiGe growth and DS)
Ni etching
Ni/Al₂O₃ (20 nm)
Guard ring etch
Electrode deposition
Back contact

Fig. 2. The processing flow and device structure of DS NiGe/Ge junctions.

First step in the fabrication process:

- Pre-cleaning of Ge
- Field oxide (SiO₂)
- Active area etching
- Ion implantation
- Ni deposition and RTA (NiGe growth and DS)
- Ni etching
- Ni/Al₂O₃ (20 nm)
- Guard ring etch
- Electrode deposition
- Back contact

Fig. 3. The I-V characteristics of NiGe/n-Ge and NiGe/p-Ge junctions by using B-DS and P-DS technique.

Fig. 4. The I-V behaviors of P-DS NiGe/n-Ge junctions in different conditions of Vᵣ at 7 K.

Fig. 5. The fabrication process and device structures of Ge p- and n-TFETs with DS NiGe metal S/D.

NiGe metal S/D.

Fig. 6. The TEM images of the gate stack structure and the P-DS NiGe Schottky junction in the Ge pTFET.

Fig. 7. The Iₒ-Vᵣ characteristics of Ge p- and n-TFETs with DS NiGe S/D.

Fig. 8. The comparison of the Iₒ dependence on temperature for pTFET and pMOSFET.

Fig. 9. Iₒ for the Ge pTFETs and the Ge pMOSFETs with different gate length (Lₒ) at V₉-V₉=-1 V.

The comparison of the S factors of Ge pMOSFET, p- and n-TFETs with different temperatures.

Fig. 10. The impact of the EOT scaling on the electrical properties of Ge pTFETs.

Fig. 11. The Iₒ-Vᵣ curves of the Ge pTFETs at low temperatures.

Fig. 12. The comparison of S factors of Ge pMOSFET, p- and n-TFETs with different temperatures.