Extended Abstracts of the 2018 International Conference on Solid State Devices and Materials, Tokyo, 2018, pp223-224

Fabrication of InAs-on-Insulator structures by Smart Cut method with hydrogen implantation at room temperature

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Abstract

InAs-OI (InAs-on-Insulator) structures with high crystallinity are fabricated by the Smart Cut process with H^+ implantation at room temperature. It is found that (111) InAs can yield much more flat surfaces after splitting than (100). After thinning by using CMP and wet etching, 15-nm-thick InAs-OI structures are realized with high thickness uniformity.

1. Introduction

Since InAs nMOSFETs [1] and Ge pMOSFETs [2] with metal S/D can be fabricated at low temperature, 3-dimensional (3D) CMOS using monolithically-stacked III-V and Ge channels with high mobility and compact lay-out is promising logic devices for future scaled technology nodes [3, 4]. In order to realize 3D CMOS, it is important to realize high quality InAs-On-Insulator (InAs-OI) structures. However, epitaxial growth of thin InAs layers with the quality close to bulk ones is quite difficult because of the large lattice mismatch. In contrast, the Smart Cut method combining direct wafer bonding with the wafer cut process due to H ion implantation [5] is expected to realize an ultra-thin body with high crystalline quality regardless of lattice mismatch. Also, Smart Cut is one of the cost-effective methods because donor wafers can be reused.

However, there are only few reports on Smart Cut of InAs. Also, H^+ implantation only at -20˚C have been reported for InAs [6, 7]. Since H^+ implantation at room temperature can be performed by conventional ion implantation equipment, this process can reduce the cost. In this study we examine the influence of the implantation dose, the implantation rate and the surface orientation on Smart Cut of InAs. It is found that InAs-OI structures can be fabricated by Smart Cut using room temperature H^+ implantation and that flatness of InAs-OI surface is improved by (111) InAs. 15-nm-thick (111) InAs-OI structures are demonstrated.

2. Experiments and discussions

The process flow in the present study is shown in Fig. 1. Here, H^+ implantation was carried out at room temperature. A 100-nm-thick SiO_2 layer was deposited for surface protection by PECVD, followed by H^+ implantation. The H^+ implantation rate was varied between 1.5×10^{13} and 2.9×10^{12} $cm^{-2}s^{-1}$ at a fixed dose of 5×10^{16} cm^{-2}. The effect of the implantation rate on (100) InAs is shown in Fig. 2. It is observed that implantation rate of 1.5×10^{13} $cm^{-2}s^{-1}$ damaged the InAs surface, while that of 2.9×10^{12} $cm^{-2}s^{-1}$ created no damage. As a result, the lower rate of 2.9×10^{12} $cm^{-2}s^{-1}$ is suitable for direct wafer bonding of InAs.

It is known that annealing of H^+-implanted substrates creates bubbles at surfaces, which are called blisters. The generation of blisters after annealing is the evidence that implanted H atoms are properly activated inside wafers and lead to splitting after bonding. Fig. 3 shows the overview of studying generation of blisters. Here, the H^+ implantation dose was varied from 1×10^{16} to 5×10^{16} cm^{-2} for (100) InAs substrates, as shown in Fig. 4, at a fixed implantation rate of 2.9×10^{12} $cm^{-2}s^{-1}$ and a fixed implantation energy of 40 keV. In addition, (111)A and (111)B surface orientations were also used at a dose of 5×10^{16} cm^{-2} for comparison. It was found that the (100) InAs surfaces only with a dose of 5×10^{16} cm^{-2} yield blisters after annealing at 170˚C for more than 5 hours, suggesting that the H^+ dose of 5×10^{16} cm^{-2} is needed to create splitting. On the other hand, blisters were generated after an ALD process at 150 ˚C for 20 min, which is much shorter than 5 hours. This fact indicates that blisters tend to occur under vacuum and that ALD process cannot be employed for InAs substrates after H^+ implantation.

Thus, H^+-implanted InAs wafers were directly bonded on Al_2O_3 on Si substrates. Al_2O_3 with the thickness of 5 to 10 nm was deposited on SiO_2/Si substrates by ALD at 300 ˚C. SiO_2 layers on InAs were etched by BHF. After performing UV/O_3 cleaning and ultrasonic cleaning for both H^+-implanted InAs and Al_2O_3/SiO_2/Si substrates, the InAs donor wafers was manually bonded to the Si handle wafers, followed by annealing at 100˚C for 24 hours and, successively, at 200˚C. The annealing at 100˚C for 24 hours has two roles; one is the increase in the bonding strength and the other is the generation of cores, so-called platelets, for splitting [8]. Fig. 5 shows a photograph of a (100) InAs-OI substrate on an entire 2-inch Si wafer, fabricated under the dose of 5×10^{16} cm^{-2}.

While (111)A and (111)B InAs can also successfully produce InAs-OI structures, the significant difference in the blister size and surface morphology after splitting was observed between (100) and (111) InAs. It is observed in Fig. 6 that the blisters on the (111) InAs are 10 times larger than on (100). Fig. 7 shows AFM images after splitting. A (100) InAs-OI surface has much larger roughness with RMS of 32 nm than (111) InAs-OI with RMS of 13 nm, suggesting the larger blisters in (111) can produce smoother surfaces after splitting. Fig. 8 summarizes the measured RMS values in comparison with the previous reports on other materials. A general trend of much smoother surfaces for (111) is confirmed. Also, no difference between (111)A and (111)B is observed. As a result, (111) InAs is advantageous in terms of flat and uniform InAs-OI formation.

The surfaces of InAs-OI were planarized by CMP with 15-nm SiO_2 abrasive for 30~40 min. Fig. 9 shows an AFM image of (111)A InAs-OI after CMP. RMS after CMP is as small as 1.0 nm. (111) InAs-OI was then thinned down to 30~10 nm with a H_2SO_4-based solution. Transmission electron diffraction and microscopy images (Fig. 10) show that the InAs layer has good crystallinity, smooth surface, and high uniformity. Since (111) InGaAs MOS interfaces have higher mobility than (100) [9, 10], ultrathin-body (111) InAs-OI channels fabricated by Smart Cut are quite promising for the aiming MOSFET application.

3. Conclusions

We have realized InAs-OI structures on entire 2-inch Si wafers by the Smart Cut process under the optimized conditions of H^+ implantation at room temperature. (111) InAs-OI

after splitting has the much smoother surface than (100) InAs-OI. Thinning by CMP and wet etching has successfully realized 15-nm-thick InAs-OI structures with smooth surfaces, high uniformity and good crystalline.

Acknowledgements This work was supported by JSPS KAKENHI Grant Number 16H06148 and JST-CREST Grant Number JPMJCR1332, Japan.

References [1] S. Kim *et al.*, IEEE Trans. Electron Dev. **60**, 3342 (2013) [2] T. Maeda *et al.*, IEEE Electron Dev. Lett. **26**, 102 (2005) [3] T. Irisawa *et al.*, *VLSI Symp.* (2014) 1. [4] V. Deshpande *et al.*, Tech. Dig. IEDM (2015) 209. [5] B. Aspar *et al.*, Journal of Electronics Materials, **30**, p.834 (2001). [6] S. Hayashi *et al.*, *ECS Trans.* **3**, 129 (2006) [7] S. A. Dayeh *et al.*, Appl. Phys. Lett. **93,** 203109 (2008) [8] S. Hayashi *et al.,* Appl. Phys. Lett. **85,** p.236 (2004) [9] Y. Urabe *et al.*, Tech. Dig. IEDM (2010) 142. [10] N. Taoka *et al.*, Tech. Dig. IEDM (2011) 61.

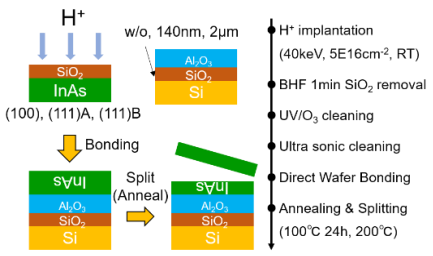

Fig. 1 Overview of Smart Cut process of InAs

Dose (cm^{-2})	5×10^{16}	
Rate ($H^+/cm^2/s$)	2.9×10^{12}	1.5×10^{13}
Surface damage post implantation	○	×

Fig. 2 Relationship between the implantation rate and the surface damage of (100) InAs

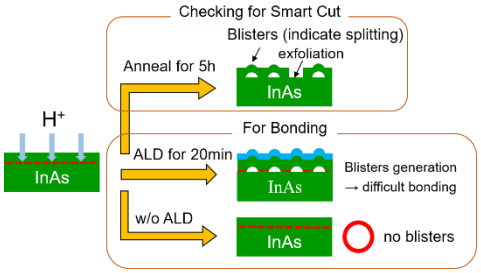

Fig. 3 Overview of blisters and effect of annealing at 170˚C and an ALD process (150˚C, 20 min) on blisters in the case of (100) InAs

Blister generation (◎: size is large)				Smart Cut
Dose ($\times 10^{16} cm^{-2}$)	1	3	5	5
(100)	×	×	○	○
(111)A	—	—	◎	◎
(111)B	—	—	◎	◎

Fig. 4 The implantation dose and the surface orientation dependence of blisters and Smart Cut

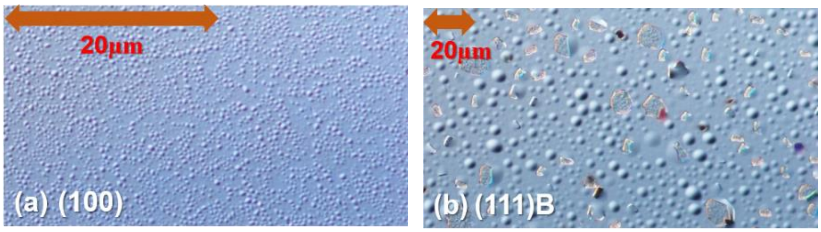

Fig. 6 Blisters on (a) (100) InAs (b) (111)B InAs substrates with a dose of 5×10^{16} cm^{-2} after annealing

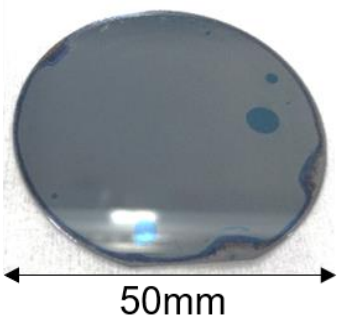

Fig. 5 (100) InAs on 140-nm-thick SiO_2 on Si after Smart Cut process

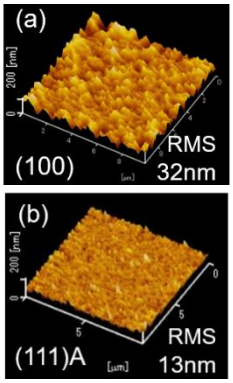

Fig. 7 10×10 μm^2 AFM images of InAs-OI after splitting, (a) (100) InAs-OI (b) (111)A InAs-OI

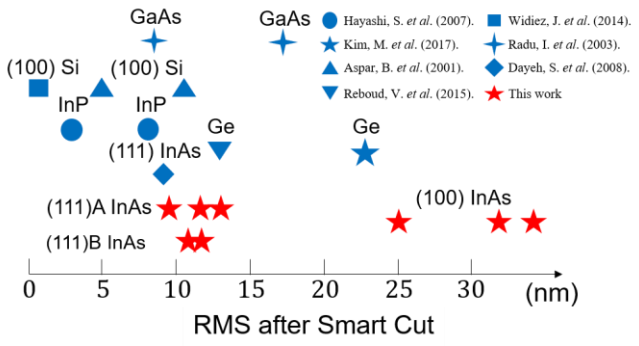

Fig. 8 Summary of surface roughness of each semiconductor after Smart Cut process

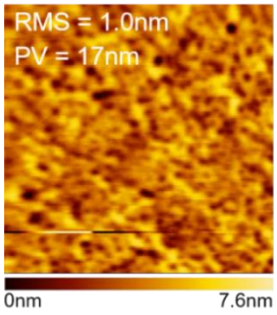

Fig. 9 10×10 μm^2 AFM image of (111)A InAs-OI after CMP

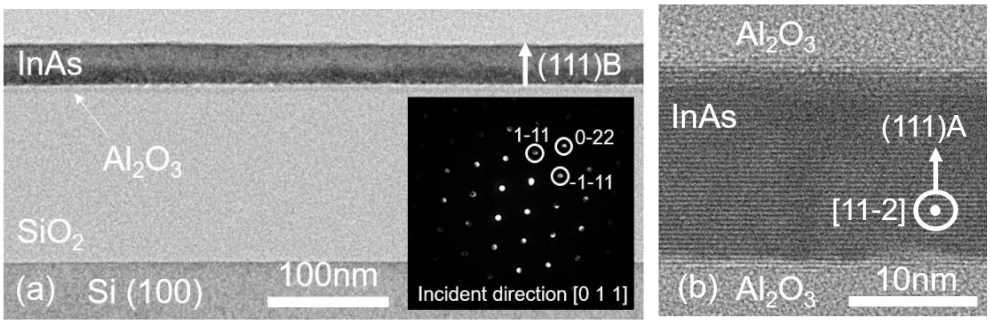

Fig. 10 Cross-sectional TEM micrograph of (111) InAs on Si substrate with 150nm-thick BOX layer after CMP and thinning with H_2SO_4-based solution. (a) 31-nm-thick (111)A InAs-OI and TED pattern of the InAs layer (b) 15-nm-thick (111)B InAs-OI