Extended Abstracts of the 2018 International Conference on Solid State Devices and Materials, Tokyo, 2018, pp225-226

In-situ plasma conditioning of InGaAs / high-κ interface layers for defect density control compatible with scalable FinFET integration

John Rozen[1], Yohei Ogawa[2], Masanobu Hatanaka[2], Takashi Ando[1], Eduard Cartier[1], Martin M. Frank[1], Marinus Hopstaken[1], John Bruley[1], Ko-Tao Lee[1], Jeng-Bang Yau[1], Yanning Sun[1], Robert L. Bruce[1], Chris D'Emic[1], Xiao Sun[1], Koukou Suu[2], Renee T. Mo[1], Effendi Leobandung[1], and Vijay Narayanan[1]

[1] IBM , T. J. Watson Research Center, Yorktown Heights, New York 10706, USA. E-mail: jrozen@us.ibm.com
[2] ULVAC, Institute of Semiconductor & Electronics Technologies, Susono, Shizuoka 410-1231, Japan

Abstract

A self-saturated plasma interlayer formed on $In_{0.53}Ga_{0.47}As$ prior to in-situ HfO_2 gate stack deposition is optimized by combining reactive species to reduce defects. It demonstrates large-scale integration compatibility from cross-wafer uniformity, three dimensional coverage and insensitivity to process queue time. Trade-off is observed between interface state density and dielectric scaling below 15Å CET. Sub-threshold slopes down to 80mV/dec are measured on 20nm gate-length FinFETs.

1. Introduction

Alternate semiconductors of the III-V family can offer fundamental benefits over Si for scaled technology nodes as they can yield higher drive currents when used as channel material in nFET devices [1,2].

Two of the many practical challenges are the reduction of electrically active defects generated at the complex compound semiconductor / dielectric interface, and the compatibility of any mitigation technique with high-volume integration tooling and environment.

Exposure of (In)GaAs surfaces to tri-methyl aluminum (TMA) as part of an Atomic Layer Deposition (ALD) process has been known to provide a self-cleaning effect of the native oxide layer [3]. More recently, it was observed that combining TMA exposure with reactive plasma species of H_2 or N_2 can yield similar benefits in scaled stacks [4,5].

In this work, we demonstrate self-limited plasma interface layer (IL) formation on $In_{0.53}Ga_{0.47}As$ yielding cross-wafer uniformity and conformality. The lowest density of interface states (D_{it}) is obtained in aggressively scaled stacks from combined reactive gas species in repeated exposure of the surface to TMA/NH_3 plasma pulses prior to in-situ HfO_2 gate dielectric deposition. The quantity measured on capacitors is correlated with the reduction of specific atomic binding configurations and its effects are directly observed in the transfer characteristics of planar and short-channel FinFET transistors.

2. Experimental

The fabrication sequence on $In_{0.53}Ga_{0.47}As$ is shown in Fig. 1. The in-situ gate stack formation is performed in an ULVAC Entron™-EX multi-chamber 300mm platform. The IL is obtained by repeated alternate exposure of precursor and reactive gas species energized by remote plasma (H_2, N_2 or NH_3). Thermal oxide ALD deposition is then achieved by using H_2O-based halide or metal-organic processes. Different test-beds are used for electrical characterization in planar capacitors and long-channel transistors. FinFET short-channel fabrication is described elsewhere [2].

X-ray photoelectron spectroscopy (XPS) in Fig. 2 reveals the self-saturated nature of the plasma IL from the Al & N signals versus TMA/N^* (N_2 plasma) cycles. The process parameters (gas, power, temperature, time…) are adjusted to minimize N incorporation and eliminate As-O, As-As, and In-O at the interface which are associated with electrically active defects. The combined reactive species in TMA/NH^* (NH_3 plasma) is found to be most efficient.

High-resolution Transmission Electron Microscopy (TEM) and Secondary Ion Mass Spectrometry (SIMS) confirm the different IL compositions found to be 10 to 20Å thick. The TMA/NH^* IL shows a higher Al to N ratio in what is confirmed to be a AlON (Fig. 4). The self-saturated nature of the IL is correlated with scavenging of the oxygen in the native $In_{0.53}Ga_{0.47}As$ surface oxide which formed following the pre-clean in etching chemistry. This enables good cross-wafer uniformity and 3D sidewall coverage around a Fin architecture (Fig. 3).

D_{it} in n-type capacitors is extracted from the 100 kHz conductance. Relative D_{it} changes correlate with measured sub-threshold slopes in our FETs. Using anneals and mitigating interface state generation, we extract values as low as $6.6\times10^{11}cm^{-2}eV^{-1}$ [6]. D_{it} varies by an order of magnitude with different plasma conditions (Fig. 5). Notably, there is a trade-off between D_{it} reduction and capacitance scaling. From leakage, frequency dispersion and hysteresis, this does not appear to be related to a secondary effect such as border traps but rather to actual dielectric constant or thickness scaling. TMA/NH^* shows the lowest D_{it} value among plasma ILs and is comparable to the thermal Al_2O_3 IL control (see matching C–V curves in Fig. 6 – left). When scaling the top HfO_2 to 20Å on that IL, Capacitance Equivalent Thickness (CET) of 13.8Å at +1V is obtained (not shown).

The optimized TMA/NH^* IL was tested in planar long channel (10μm) and FinFET short channel (20-30nm) transistors. Both show a good yield and down to 80mV/dec sub-threshold slope, at V_d = 50mV, matching the control (see Fig. 7 – left). The cross-wafer thickness uniformity is verified by the leakage current distribution (Fig. 7 – right). Finally, the best short channel devices show no clear sensitivity to queue time between the wet pre-clean and the gate stack deposition (Fig. 6 – right).

3. Conclusions

A plasma IL was demonstrated to be scalable to wafer-level short-channel FinFET integration. The scavenging of surface oxygen was optimized to reduce D_{it} and improve the transfer characteristics. The optimized plasma process using combined reactive species provides a significant pathway decouple the wet pre-clean and the gate modules.

Acknowledgements

We thank T. C. Chen (IBM); T. Kondo, K. Saito, H. Obinata and S. Iwashita (ULVAC) for their continuous executive support. We acknowledge the technical contribution from IBM's Microelectronics Research Lab and ULVAC's field service teams.

References

[1] Y. Sun *et al., International Electron Devices Meeting* (2014) 582.

[2] X. Sun *et al., Symposium on VLSI Technology* (2017) T40.

[3] M. Frank *et al*., Appl. Phys. Lett. **86** (2005) 152904.

[4] A. Carter *et al.,* Appl. Phys. Express **4** (2011) 091102.

[5] V. Chobpattana *et al.,* Appl. Phys. Lett. **102** (2013) 022907.

[6] E. Cartier *et al., International Reliability Physics Symposium* (2018) 5A.4.

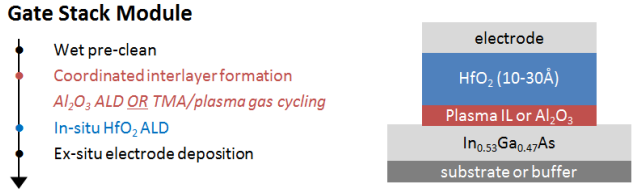

Fig. 1 Process flow for all samples. Plasma gas: H_2, N_2 or NH_3

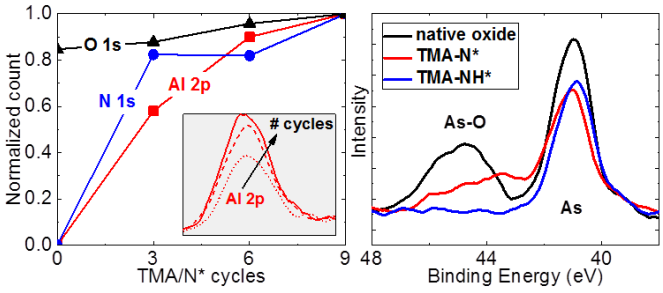

Fig. 2 XPS data showing self-saturation in TMA/N* (left) and benefit of TMA/NH* showing As-O reduction (right)

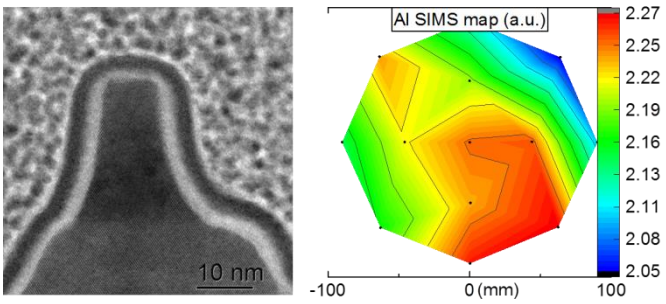

Fig. 3 TMA/NH* IL conformality (left - InGaAs Fin coverage w/ HfO_2 top layer) and uniformity (right - 200mm SIMS Al map)

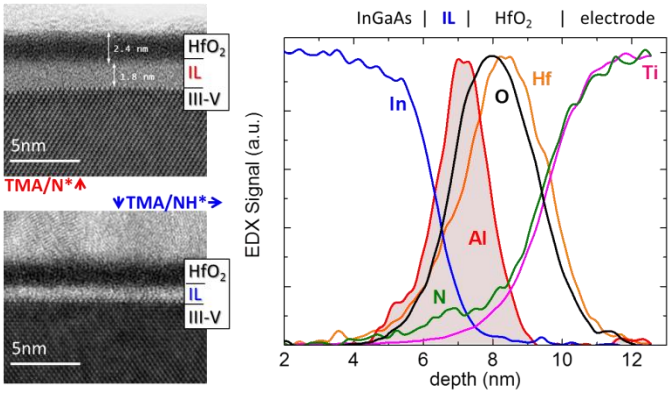

Fig. 4 TEM images and EDX profiles of the plasma ILs

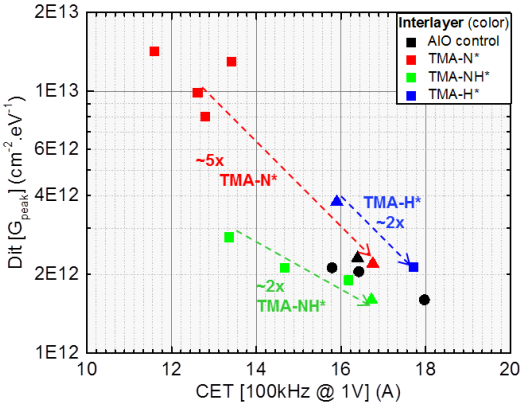

Fig. 5 D_{it} reduction over plasma IL process space & scaling trade-off observed in capacitance-equivalent thickness at 1V

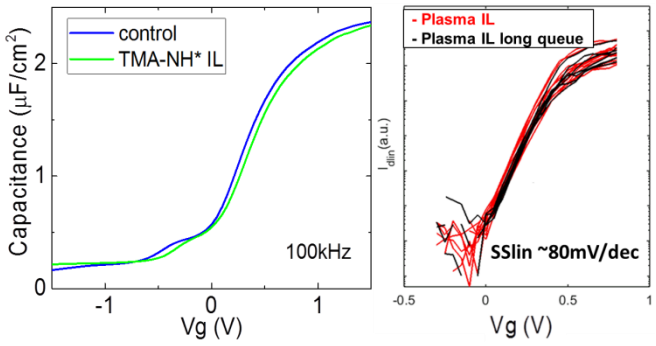

Fig 6 C–V curves on MOSCAPs (left) and negligible post-wets queue time impact on Id-Vg in 30nm FinFETs w/ plasma IL (right)

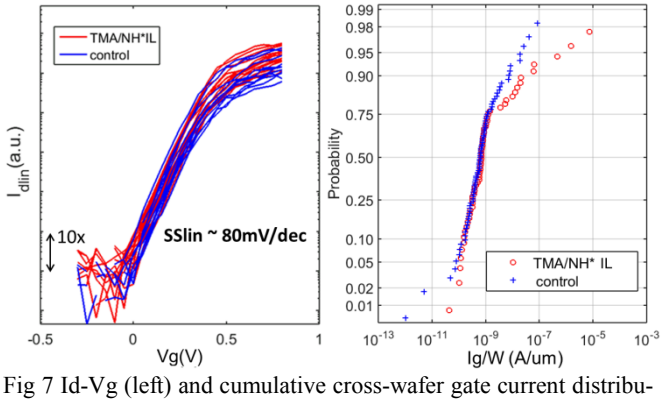

Fig 7 Id-Vg (left) and cumulative cross-wafer gate current distribution (right) of plasma IL vs. control in 30nm gate-length FinFETs