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Suppression of Band-to-Band Tunneling in III-V MOSFETs on Silicon Using Source and Drain Spacers

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Abstract--In this work, we demonstrate InGaAs planar FETs and FinFETs integrated on silicon substrates. In InGaAs FETs, the relatively large off-current caused by the narrow band gap represents a key issue. We report here that the use of SiN_x spacers between the source/drain and the gate significantly reduces the off-current through suppression of band-to-band tunneling and the parasitic bipolar effect. Using this technology, we achieve record on-current of 280 µA/µm at I_{OFF} = 100 nA/um and V_{DD} = 0.5 V for a scaled III-Vs FET on Si.

1. Introduction. High electron mobility III-V materials such as InGaAs are promising candidates as replacement for Si beyond the 7 nm node [1]. One of the key challenges of III-V FETs is the reduction of the relatively high off-current, I_{OFF}, caused by band-to-band tunneling (BTBT) due to a narrow band gap [2]. Moreover, the III-V channel must be integrated on a Si substrate. This can be done e.g. through direct wafer bonding, which additionally supplies a buried oxide layer (BOX) back-barrier for enhanced electrostatic confinement [3]. The floating body of such a structure, however, is considered to cause the parasitic bipolar effect (PBE), accumulation of holes in the channel, which further amplifies I_{OFF} [4]. In this work, we demonstrate InGaAs planar FETs and FinFETs integrated on Si substrates. To reduce I_{OFF}, SiN_x spacers are implemented between the gate and the source/drain. Devices with spacers show significantly lower I_{OFF}, which allows the on-current at fixed I_{OFF} to reach record values.

2. Experimental. Device fabrication starts by direct wafer bonding of a 20-nm thick InGaAs layer on a Si wafer. More details about the process flow can be found elsewhere [5]. Following, fins are patterned and etched by reactive ion etching (RIE) with inductively coupled plasma. A replacement metal gate (RMG) process is utilized, starting with deposition and patterning of the dummy metal gate. Subsequently, 4 nm wide SiN_x spacers are deposited by PECVD and patterned in a self-aligned manner by RIE. MOCVD regrowth of *in situ* doped n^+ raised source and drain (RSD) contacts follows. After deposition of an interlayer dielectric, planarization by CMP and removal of the dummy gate is performed. A bilayer high-k (Al_2O_3/HfO_2, EOT ~ 1 nm) dielectric and gate metal (TiN) is deposited on the InGaAs channel. After a second planarization step, the contact vias are opened and metallized with W. FinFETs and planar FETs with gate length, L_G, down to 15 nm and fin widths, W_{fin}, down to 30 nm are characterized in this work.

3. Results. Fig. 1a shows subthreshold characteristics of FinFETs with W_{fin} = 30 nm and L_G = 15 nm. With spacers, I_{ON} = 280 µA/µm (I_{OFF} = 100 nA/µm, V_{DD} = 0.5 V), SS_{sat} = 79 mV/dec., SS_{lin} = 70 mV/dec. and DIBL = 25 mV/V is achieved. The use of spacers causes an increase of R_{ON} at long L_G (Fig. 1b). This is due to increased R_{access} from the ungated regions under the spacers. However, for L_G < 30 nm, devices without spacers suffer from short-channel effects which effectively increase R_{ON}, making the use of spacers superior for these gate lengths. Fig. 2 shows I_{OFF}, defined as min(I_{DS}), versus L_G for FinFETs and planar FETs. For FinFETs, I_{OFF} is approximately constant at L_G > 1 µm, while it significantly increases at scaled L_G. This is consistent with the PBE [4]. At L_G < 30 nm, the use of spacers reduces I_{OFF} by approximately two orders of magnitude. The increase of I_{OFF} versus V_{DS}, as shown in the inset, is a strong indicator of BTBT. Fig. 3 shows I_{ON}/I_{OFF} versus L_G. Here, I_{ON} is defined as I_{DS} at V_{GS} - V_T = 1 V. For long L_G FETs using spacers, the reduction of I_{OFF} is balanced by a reduction of I_{ON}, while for scaled L_G, the reduction of I_{OFF} becomes significant. Fig. 4 shows I_{ON} at different I_{OFF} at a fixed V_{DD} = 0.5 V for many devices. At L_G = 50 nm, I_{OFF} is reduced by more than two orders of magnitude using spacers.

Fig. 5 shows I_{ON} (I_{OFF} = 100 nA/µm, V_{DD} = 0.5 V) versus L_G with and without spacers. Even at fixed I_{OFF} = 100 nA/µm, the reduced minimum I_{OFF} through the use of spacers enables higher I_{ON} due to a steeper SS near the I_{OFF} target. Fig. 6 shows a benchmark of scaled III-V-on-Si FETs. The I_{ON} = 280 µA/µm (at I_{OFF} = 100 nA/µm and V_{DD} = 0.5 V) reported here represents the highest value for devices with L_G < 50 nm.

4. Conclusions. We have demonstrated InGaAs-on-Si MOSFETs, which implement SiN_x source/drain spacers to reduce the effect of BTBT and the PBE, resulting in devices with record I_{ON} of 280 µA/µm for scaled III-V-on-Si FETs, showing the potential of S/D spacers in these kinds of devices.

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References

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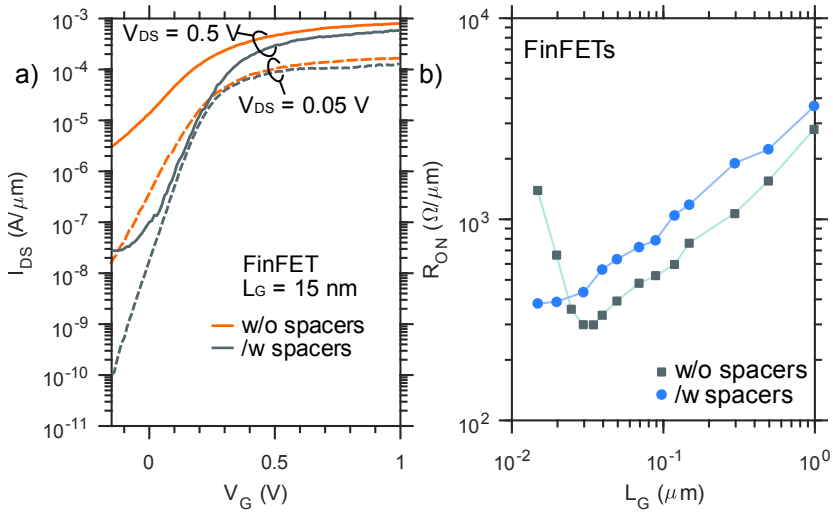

Figure 1 (a) Subthreshold characteristics of L_G = 15 nm FinFETs with and without spacers. At V_{DS} = 0.5 V, the former exhibits a two order of magnitude reduction of I_{OFF}, enabling an I_{ON} of 280 μA/ μm at I_{OFF} = 100 nA/μm and V_{DD} = 0.5 V. (b) R_{ON} versus L_G with and without spacers. At long L_G, devices with spacers exhibit higher R_{ON} due to the increased access resistance under the spacer regions. At short L_G, devices without spacers exhibit higher R_{ON} because of the high output conductance due to BTBT.

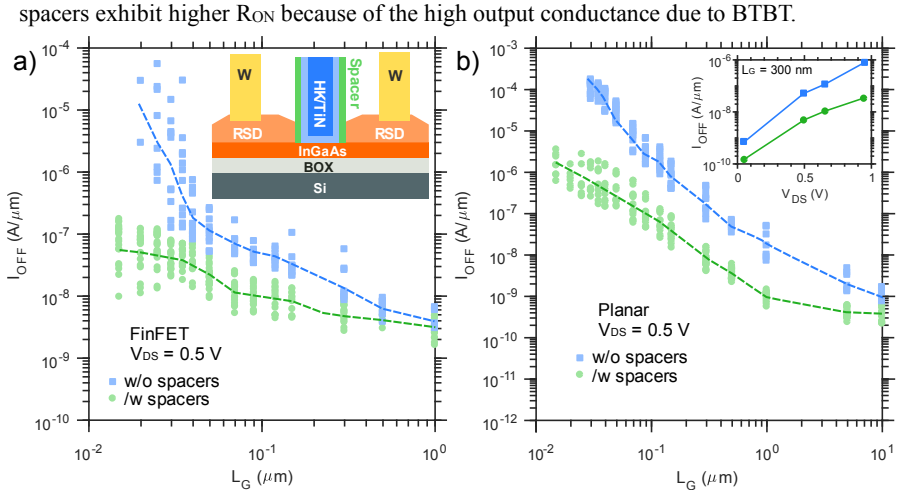

Figure 2 I_{OFF}, defined as the minimum value of I_{DS}, versus L_G with and without spacers for (a) FinFETs and (b) planar devices. At long L_G, I_{OFF} remains approximately constant, while it increases steeply for scaled L_G, which is a sign of the parasitic bipolar transistor effect. For FinFETs, the use of spacers offers a strong reduction of I_{OFF} at L_G = 30 nm and below. Left inset shows a schematic of the device structure. Right inset shows I_{OFF} versus V_{DS}, the trend is indicative of band-to-band tunneling.

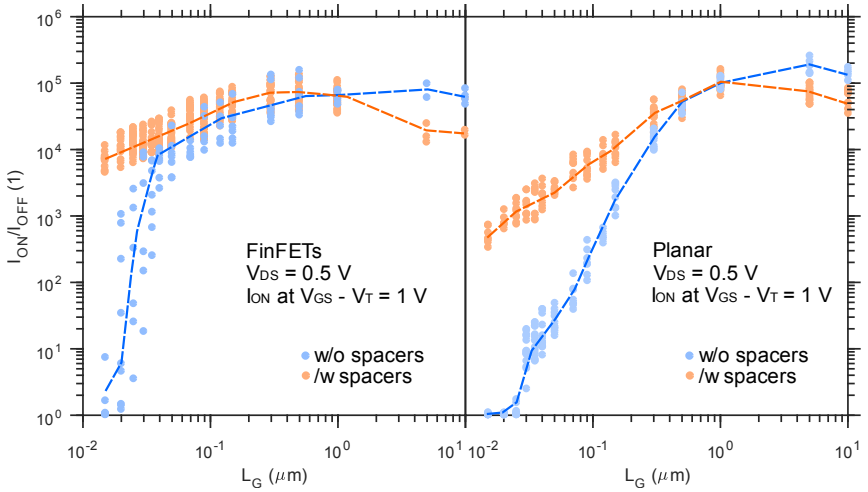

Figure 3 I_{ON}/I_{OFF} versus L_G. Here, I_{ON} is defined as I_{DS} at V_{GS} - V_T = 1 V. At long L_G, I_{ON}/I_{OFF} remains approximately constant with and without spacers due to the reduction of I_{OFF} being balanced by a reduction of I_{ON} in the latter.

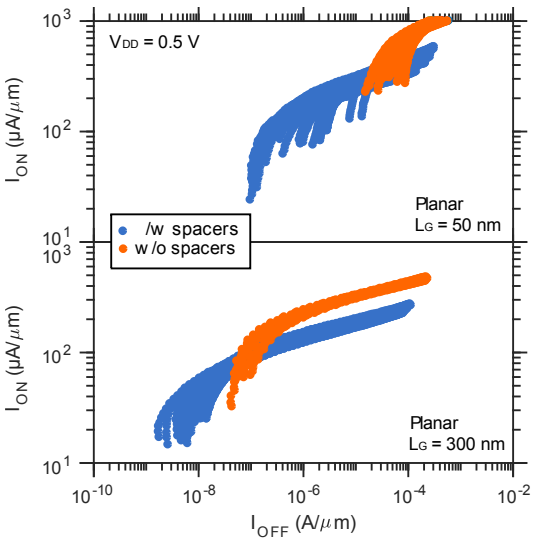

Figure 4 I_{ON} at fixed V_{DD} of 0.5 V and variable I_{OFF}. For large I_{OFF}, devices without spacers exhibit larger I_{ON} due to lower R_{ON}. Scaled devices however are unable to reach very small I_{OFF} without spacers.

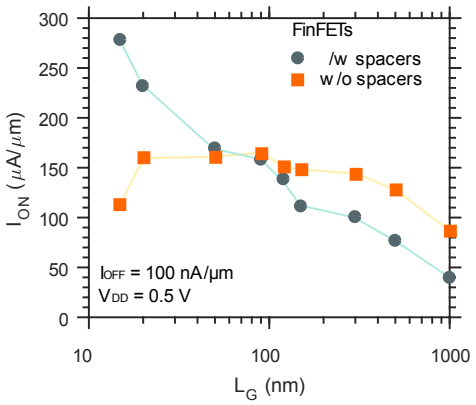

Figure 5 Peak values of I_{ON} versus L_G with and without spacers. Using spacers significantly enhances I_{ON} at scaled L_G due to reduction of the minimum I_{OFF}. This results in a steeper SS near the target I_{OFF} of 100 nA/μm. At long L_G, the increased R_{access} due to spacers reduces I_{ON}.

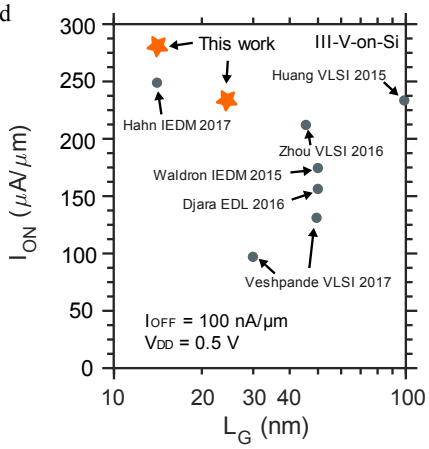

Figure 6 Benchmark of I_{ON} for state-of-the-art III-V-on-Si MOSFETs at L_G < 100 nm. The devices reported in this work represent the highest performing such devices, in particular at the technologically relevant L_G < 20 nm. This is enabled by the S/D spacers reducing I_{OFF}.