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Comprehensive Study of Variability in Poly-Si Channel Nanowire Transistor ~ Grain Boundary effect in Variability ~

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Abstract

Variability in poly-Si nanowire transistors (NW Tr.) is studied with respect to device and grain size. Threshold voltage (V_{th}) variability decreases as grain size or nanowire width (W) decreases since the number of grain boundaries in carrier passage increases. Drain current (I_d) variability shows similar grain size and W dependences, while I_d variability in short channel Tr. is suppressed due to the parasitic resistance. In addition, I_d variability decreases with high lateral or perpendicular electric field due to potential barrier lowering at grain boundaries.

1. Introduction

Poly-Si has become a key channel material for 3D LSIs [1-6]. Compared to single crystalline-Si Tr., one of the key issues of poly-Si Tr. is the variability due to the random potential barrier at grain boundaries. Although the variability in poly-Si channel with vertical FET has been reported [5], the relation between device and grain size has not been clarified since it is difficult to investigate the size dependence in vertical FET. In this paper, we study the grain and device size dependence of V_{th} and I_d variability.

2. Device fabrication

Fig.1 shows the schematic and TEM image of poly-Si NW Tr. fabricated on a 300mm wafer. Gate stack consists of poly-Si gate and SiO_2 gate oxide. In order to reduce the parasitic resistance, source and drain (S/D) were elevated by Si-epitaxial growth. For the comparison, single-crystalline-Si NW Tr. was also fabricated from SOI wafer (SOI NW Tr.). NW patterning after poly-Si crystallization annealing can attain the same grain size within a wafer. In addition to poly-Si NW Tr. with small grain by the conventional poly-Si crystallization, that with large grain was achieved by tuning crystallization annealing and poly-Si thinning processes [3]. As shown in Fig.2, higher mobility was obtained in poly-Si NW Tr. with larger grain.

3. Threshold voltage variability

Fig.3 shows gate length (L) dependence of σV_{th} in poly-Si NW Tr. with different grain size and that in SOI NW Tr. plotted against $1/(LW_{eff})^{1/2}$, where $W_{eff} = (W+2H)$. σV_{th} in poly-Si NW Tr. is much larger than that in SOI NW Tr. due to random potential barrier height at the grain boundary. In addition, σV_{th} in poly-Si NW Tr. with large grain, in spite of larger mobility, is larger than that with small grain. In poly-Si NW Tr. with small grain, the number of grain boundaries is large reducing the relative impact of potential barriers at grain boundaries leading to the small V_{th} variability [4]. Figs.4 and 5 show size dependence of σV_{th} in SOI and poly-Si NW Tr., respectively. In SOI NW Tr. with short L, σV_{th} decreases as W decreases due to the suppression of the short channel effect (SCE) by strong gate controllability (Fig.4(a)), while σV_{th} with long L increases as W decreases (Fig.4(b)) since the effect of line edge roughness becomes larger with narrower W [7]. Similarly to SOI NW Tr., σV_{th} in poly-Si NW Tr. with short L is smaller with narrower W due to SCE suppression (Fig.5(a)). Meanwhile, σV_{th} with long L dose not increase as W decreases (Fig.5(b)) where SCE is confirmed to be negligibly small by L dependence of subthreshold slopes (Fig.6). In order to investigate the origin of smaller variability in poly-Si NW Tr. with narrower W, W dependence of mobility was extracted by split C-V measurement with 1000 NWs between S/D. As shown in Fig.7, mobility decreases as W decreases. Due to the limited carrier passage with narrower W, carriers are restricted from the degree of freedom in avoiding grain boundaries along NW width direction so that the number of grain boundaries in carrier passage increases as W degreases (Fig.8). Similarly to grain size dependence, large number of grain boundaries reduces not only the mobility but also the relative impact of potential barriers at grain boundaries leading to the small V_{th} variability.

4. Drain current variability

I_d variability was compared with the same gate overdrive voltage (V_g-V_{th}) in order to eliminate V_{th} variability and was normalized by median I_d ($<I_d>$). Fig.9 shows L dependence of $\sigma I_d/<I_d>$ in poly-Si NW Tr. with different V_d. In short L, $\sigma I_d/<I_d>$ is smaller with higher V_d due to the lowered potential barrier by high lateral electric field. Furthermore, $\sigma I_d/<I_d>$ in poly-Si NW Tr, with L=100 nm is smaller than that with L=200 nm. In addition to increasing lateral electric field by reducing L, smaller $\sigma I_d/<I_d>$ with L=100nm can be explained by S/D parasitic resistance (R_{SD}). R_{on} is larger with smaller W due to the larger R_{SD} (Fig.10). R_{SD} with W=12.5nm and L=100nm covers a certain proportion of R_{on}. Due to the poly-crystallinity, poor Si-epitaxial growth at S/D might result in large R_{SD} which is about 10 times larger than R_{SD} in SOI NW Tr. Thereby, higher part of I_d distributions in L=100nm is suppressed leading to the smaller variability compared to that in L=200nm (Fig.11). Similarly to σV_{th}, $\sigma I_d/<I_d>$ in poly-Si NW Tr. is much larger than that in SOI NW Tr. and $\sigma I_d/<I_d>$ with small grain is slightly smaller than that with large grain (Fig.12). Figs.13(a) and 13(b) show V_g dependence of $\sigma I_d/<I_d>$ with short L and long L, respectively. $\sigma I_d/<I_d>$ in SOI NW Tr. is independent of V_g, while that in poly-Si NW Tr. decreases with increasing V_g. As well as V_d dependence of $\sigma I_d/<I_d>$, high perpendicular electric field by large V_g lowered potential barrier at grain boundaries leading to the smaller $\sigma I_d/<I_d>$. In addition, strong V_g dependence of $\sigma I_d/<I_d>$ in short L is due to suppressed I_d variability by R_{SD} with high V_g since impact of R_{SD} becomes larger with higher V_g.

5. Conclusion

Fig.14 summarized grain and device size dependence of variability in poly-Si NW Tr. Smaller grain leads to lower mobility, whereas the variability in both V_{th} and I_d are suppressed. Due to the limited carrier passage, number of grain boundaries in poly-Si NW Tr. increase as W decreases leading to the slight decrease in mobility and variability. In short L, variability was enhanced due to SCE, while it can be suppressed with narrower W. Although large R_{SD} in narrow W and short L is the disadvantage of I_{on}, I_d variability was found to be suppressed. Therefore, scaled poly-Si NW Tr. with small grain is effective to suppress variability in spite of I_{on} degradation. These results can give the guideline for the practical use of poly-Si channel in 3D applications.

References

[1] C. -C. Yang et al., IEDM2013, p.731. [2].M. Saitoh et al., VLSI2014, p.178. [3] M. Oda et al., IEDM2015, p.125. [4] M. Toledano-Luque et al., IEDM2012, p.203. [5] D. Resnati et al., IEDM2017, p.103. [6] A. Subrits et al., IEDM2017, p.517. [7] M. Saitoh et al., VLSI2011, p.132.

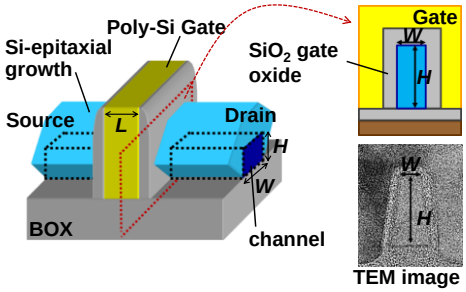


Fig.1 Schematic and TEM image of poly-Si NW Tr. Gate stack consists of poly-Si gate and SiO_2 gate oxide.

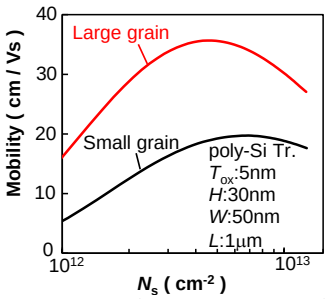


Fig.2 Mobility of poly-Si Tr. with different grain size. Higher mobility was obtained with larger grain.

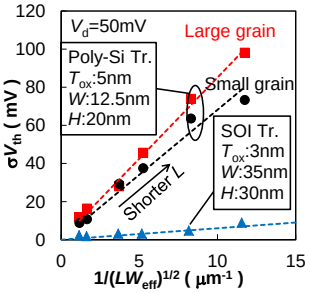


Fig.3 L dependence of σV_{th} in poly-Si NW Tr. with different grain size and SOI NW Tr. plotted against $1/(LW_{eff})^{1/2}$.

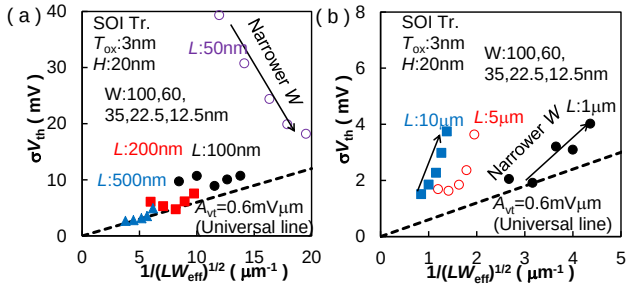


Fig.4 Size dependence of σV_{th} in SOI NW Tr. (a) with short L and (b) long L. σV_{th} with short L decreases as W decreases due to the suppression of SCE, while σV_{th} with long L increases as W decreases due to line edge roughness.

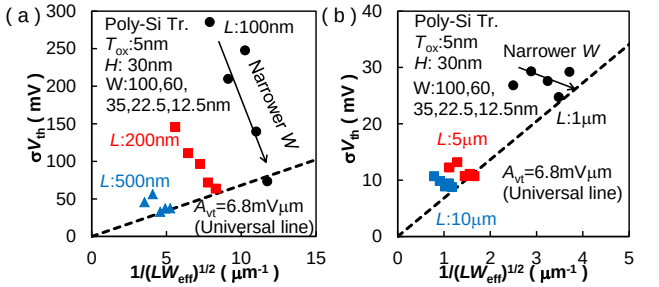


Fig.5 Size dependence of σV_{th} in poly-Si NW Tr. (a) with short L and (b) long L. σV_{th} dose not increase with the decrease of W in poly-Si NW Tr. with long L.

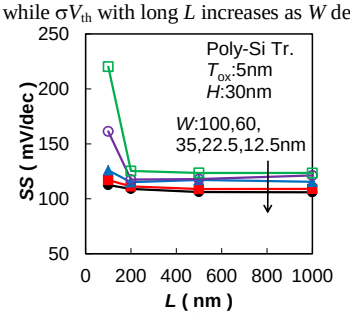


Fig.6 L dependence of Subthreshold slope. SCE is negligible for L >200 nm.

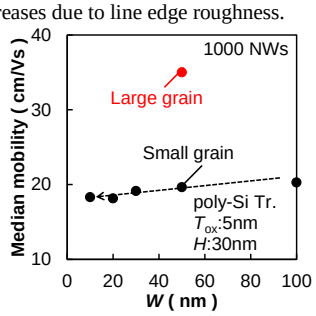


Fig.7 W dependence of mobility. Mobility is larger with larger grain size and decrease with W.

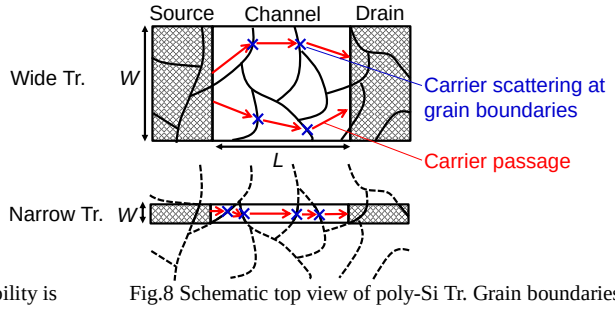


Fig.8 Schematic top view of poly-Si Tr. Grain boundaries increases as W decreases due to limited carrier passage.

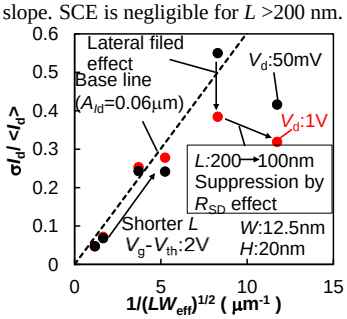


Fig.9 L dependence of $\sigma I_d/\langle I_d\rangle$ in poly-Si NW Tr. with different V_d. $\sigma I_d/\langle I_d\rangle$ is smaller with higher V_d.

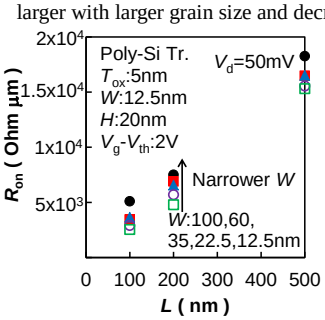


Fig.10 R_{on}-L in poly-Si NW Tr. with different W. R_{on} is larger with smaller W due to larger R_{SD}

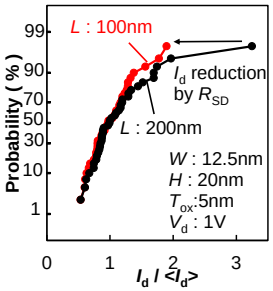


Fig.11 $I_d/\langle I_d\rangle$ distributions in poly-Si NW Tr. with L=100nm and L=200nm.

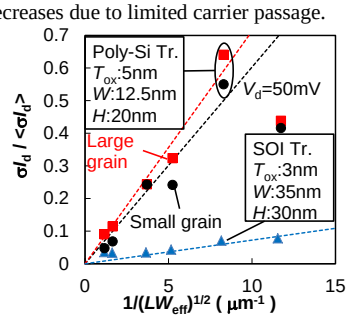
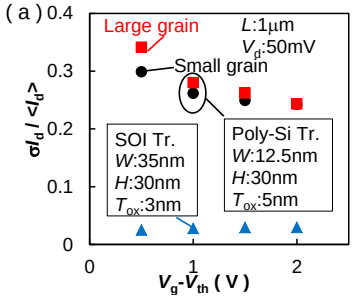


Fig.12 L dependence of σ $I_d/\langle I_d\rangle$ in poly-Si NW Tr. with different grain size and SOI NW Tr.



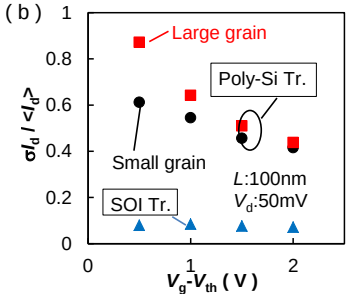


Fig.13 V_g dependence of $\sigma I_d/\langle I_d\rangle$ with (a)long L and (b) short L. Larger V_g lowered potential barrier at grain boundaries leading to the smaller $\sigma I_d/\langle I_d\rangle$.

	Larger grain(median) 243nm →111nm	Narrower W 100nm →12.5nm	Shorter L 200nm →100nm
On-current	Mobility decrease (-44% in mobilty)	Mobility decrease (-10% in mobility)	Suppressed by R_{SD} (-20% in I_{on}*L)
Variability	Increase grain boundaries and samller relative inpact of potential barriers (-20% in A_{Vt}, -16%in A_{Id})	Suppression of SCE in short L (-25% in σV_{th} @ L =100nm)	Enhanced SCE in wide W (+96% in σVth @ W=100nm)
		Increase grain boundaries (-18% in σVth @ L =10μm)	R_{SD} effect in narrow W (-24% in $\sigma I_d/\langle I_d\rangle$ @ W=12.5nm)

Fig.14 Summary of grain and device size effect on variability. Scaled poly-Si NW Tr. with small grain is effective to suppress variability in spite of I_{on} degradation.