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Novel Vertical GaN Power Devices

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Abstract

Vertical gallium nitride (GaN) power devices have attracted increased attention due to their superior high-voltage and high-current capacity as well as easier thermal management than lateral GaN high electron mobility transistors. Vertical GaN devices are promising candidates for next-generation power electronics in electric vehicles, data centers, smart grids and renewable energy processing. This talk illustrates our recent progress in developing vertical GaN power devices, including the demonstration of vertical GaN fin power field-effect-transistors (FETs) with a record power device figure of merit (Baliga's FOM), wafer-level vertical GaN power devices by controlled spalling, as well as vertical GaN power devices on low-cost substrates. These results demonstrate the great potential of vertical GaN power devices for next-generation high-voltage and high-current power switching applications.

1. Introduction

The availability of low-cost, efficient and reliable power switching devices is central to improving the efficiency of power electronics. GaN-based transistors and diodes are exciting candidates for next-generation power electronics. Currently, both lateral and vertical structures are considered for these GaN power devices. In particular, vertical GaN power devices have attracted significant attention thanks to their capability of achieving high breakdown voltage (*BV*) and current levels without enlarging the chip size, the superior reliability gained by moving the peak electric field away from the surface into bulk devices, and the easier thermal management [1] than lateral devices.

This talk will review some of the novel material-, device- and wafer-level technologies that have been recently developed for a new-generation of high-performance and low-cost vertical GaN power devices.

2. Experimental Results

Traditional GaN-based vertical transistors are based on two different technologies: current-aperture vertical electron transistor (CAVET) [2-3] and trench MOSFETs [4]. Despite the excellent performance demonstrated by these transistors, the development of vertical GaN power transistors has been hindered by the complex fabrication technology required by both the CAVET and the trench MOSFET structures, namely the requirement for epitaxial regrowth or p-type GaN. The epitaxial regrowth (e.g. required for CAVETs) greatly increases the complexity and cost of device fabrication, and it also makes it difficult to achieve normally-off operation. At the same time, an inverted channel on p-type GaN, as required for fabricating trench MOSFETs, has very low carrier mobility and typically suffers from traps and defect states.

To overcome these challenges, our group recently demonstrated a novel device structure, the GaN vertical fin power FET [5-6]. This transistor only needs the growth of n-GaN layers, no need for p-GaN or epitaxial regrowth. In this device (Fig. 1), the current is controlled through sub-micron-fin-shaped vertical n-GaN channels, which are surrounded by gate dielectrics and metal electrodes. At zero gate bias, the electrons in the fin channels are depleted due to the work function difference between the gate metal and GaN. By shrinking the fin width below 500 nm, this full fin-channel depletion induces a normally-off transistor operation. A specific on-resistance (R_{on}) of 0.2 mΩ·cm^2 was demonstrated for a breakdown voltage over 1200 V, rendering a Baliga's FOM of 7.2 GW/cm^2, a record for all vertical GaN power transistors. These devices also showed a threshold voltage of 1 V was achieved and was stable up to 150 °C.

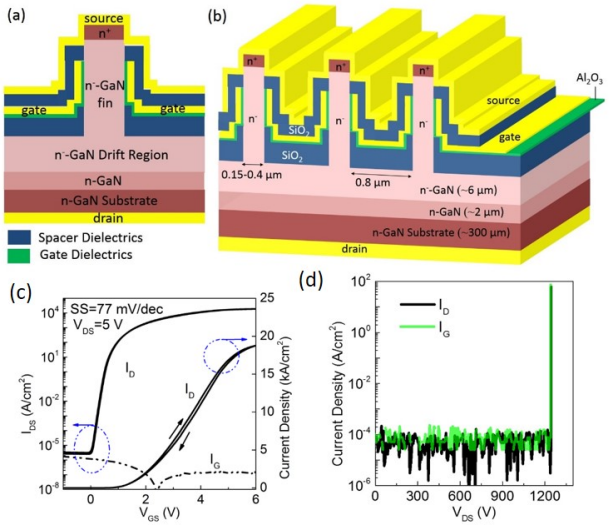

Fig. 1. (a) Cross-sectional schematic of a device fin unit-cell and (b) side-view 3-D schematic of vertical GaN fin power FETs. (c) Double-pulse forward transfer curves and (d) reverse characteristics of the fabricated vertical GaN fin power FETs.

Despite the high performance demonstrated in vertical GaN power devices, their commercialization is hindered by the high cost of bulk GaN substrates used in these devices. Recently, our team demonstrated successful wafer-scale layer transfer from 2-inch diameter bulk GaN substrates by using a novel technique called Controlled Spalling [7] (Fig. 2). This technique allows for wafer-level device transfer of vertical GaN power devices and the re-use of GaN substrates for epitaxy growth, such to greatly reduce the device cost. This technology was applied to the transfer of 600-1200 V class vertical GaN power diodes from bulk GaN substrates to Si substrates. The transferred diodes showed a reduced R_{on}, due to the reduction in substrate resistance, and no degradation in device *BV* and off-state leakage. We are currently working on the wafer-level transfer of vertical GaN fin power FETs.

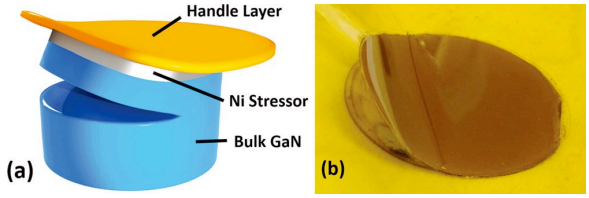

Fig. 2. (a) Illustration depicting the Controlled Spalling process for bulk GaN substrates and (b) an image of 2-inch bulk GaN wafer during the spalling processing. The figure source is [7].

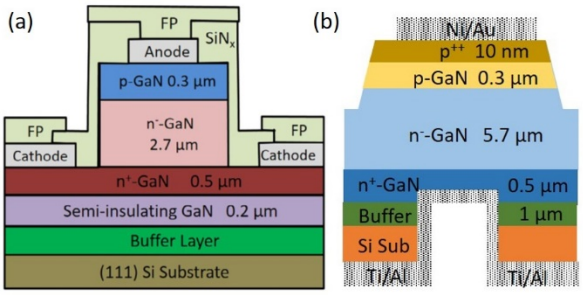

Fig. 3. Schematics of (a) quasi-vertical GaN-on-Si power diodes [8-9] and (b) fully-vertical GaN-on-Si power diodes [10].

An alternative approach that can fundamentally circumvent the high cost of today's vertical GaN devices is to fabricate them directly on Si substrates, which allow almost 100-fold lower wafer and epitaxial cost as well as 8-inch fabrication. However, the insulating buffer layers present in the GaN-on-Si wafer and the relatively high dislocation density in GaN make it challenging to demonstrate vertical GaN-on-Si power devices. By overcoming these challenges, we demonstrated the world's first GaN-on-Si vertical power diodes in 2014 [8-9], by utilizing a quasi-vertical structure where the anode and cathode were formed on a mesa structure on the same side of the wafer (Fig. 3(a)). Recently, we demonstrated fully-vertical GaN-on-Si power diodes by selective removal of Si substrates and buffer layer [10] (Fig. 3(b)). This fully-vertical diode exhibited a specific R_{on} of 0.35 mΩ·cm^2 and a *BV* of 720 V, rendering a record Baliga's FOM in all vertical GaN power diodes on foreign substrates as well as significantly better performance than commercial Si and SiC power diodes at a breakdown voltage. Besides, we identified the design space of vertical GaN power diodes on different substrates [11-12]. These results demonstrated the great potential of low-cost vertical GaN-on-Si diodes for 600-V class power switching applications, and helped to pave the way to demonstrate low-cost fully-vertical GaN-on-Si power transistors.

3. Conclusions and Outlook

Vertical GaN power devices are exciting candidates for next-generation medium- and high-voltage (over 650 V) and high-current (over 100 A) power switching applications in electric vehicles, smart grids and renewable energy processing. Remarkable progress in material epitaxy, device design and fabrication, as well as wafer-level processing technologies has been achieved in these devices. At the same time. exciting research opportunities are still open in wafer-level device transfer, thick GaN epitaxy on Si, device breakdown physics, device reliability and circuit-level applications. Commercially-viable vertical GaN vertical power devices delivering excellent performance and low cost could be a reality for high-power applications in the next five to ten years.

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