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A Compact Model of MOS Capacitors Taking Deep Level Trap Effects into Account

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Abstract

A compact model of MOS capacitors for circuit simulator is proposed which takes effects of deep level traps into account. In the model, one-dimensional Poisson and current continuity solver is coupled to equations for deep level traps by using several ten's of mesh points. The model is used in transient mode, and successes in obtaining *C-V* characteristics including their hysteresis and frequency dispersions. In the method, trap energy distribution is incorporated by defining several trap of different energy levels. Transient behaviors of all the traps coupled with carrier dynamics are successfully solved self-consistently. The proposed method can be used as a powerful tool in modeling of MOS *C-V* characteristics.

1. Introduction

GaN MOSFET is widely studied for higher speed, higher power applications [1]-[4] beyond silicon power devices. Recently good MOS *C-V* characteristics are reported [5], but it still has some restrictions. Unideal *C-V* characteristics of GaN MOS capacitors are occurred mainly by interfacial deep level traps. From experimental points of view, it is hard to distinguish such *C-V* non-ideality without any theoretical tools. In this work, a compact model using numerical method is proposed with deep level trap equations in order to obtain MOS *C-V* characteristics with hysteresis and frequency dispersions. The method is applied to GaN MOS capacitors, and benefits of the present approach in obtaining *C-V* curves with hysteresis and frequency dispersions are successfully demonstrated.

2. Physics of Deep Level Traps

Physics of deep level traps are modeled successfully in device simulation field as ref. [6] where interaction of carrier and traps are incorporated by trap rate equations (1) and (2), where only acceptor traps are considered. This rate equations differ when different energy levels are considered.

$$\frac{\partial N_{TA}^{-}}{\partial t} = E_n \cdot N_{TA}^{-} - C_n \cdot n \cdot (N_{TA} - N_{TA}^{-}) + E_p \cdot (N_{TA} - N_{TA}^{-}) - C_p \cdot p \cdot N_{TA}^{-} \quad (1)$$

$$E_n = v_{th}\sigma_n N_C exp(-q\Delta E/k_B T) \quad (2)$$

Fig. 1 schematically shows interactions of carrier and deep level traps. In case of acceptor type trap, electrons are captured in fast time scale but emitted from the trap in slower time scale depending on the energy depth. This time scale is extended over many orders of magnitude, but it is necessary to solve all the trap equations of all trap equations consistently with carrier continuity equation and Poisson equation.

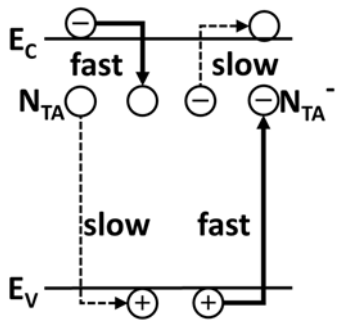

Fig. 1 Schematic view of the carrier trap dynamics related to acceptor type traps in the band gap. Carriers are fastly captured but emitted from the traps slower depending on the energy depth of the trap.

3. Numerical Method Used in the Present Method

Although it is required to solve all the equations self-consistently, it should be as compact as possible in order to be used in circuit simulation. In the present method, all equations are solved using one-dimensional approximation from substrate to insulator. This reduces the mesh points below several ten's.

Current continuity equation and trap equations include transient terms, and are discretized by the implicit method. It is also not preferable to use fully coupled form of all equations because the matrix becomes too large. Therefore we use iterative solutions of equations de-coupled from each other. Because of the implicit formulation of the transient term, consistency of all equations are obtained after the iterative decoupled solution is converged for one time step. Fig. 2 shows an example of C-V curve without any traps.

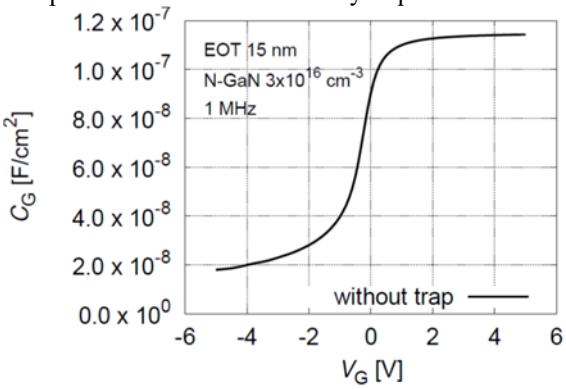

Fig. 2 *C-V*-curve for a GaN MOS capacitor without any interface trap calculated by the present method. Oxide thickness is assumed to be 15 nm.

4. Impact of Interface Traps on MOS C-V curves

The present method is applied to GaN MOS capacitors in order to obtain various types of unideal *C-V* curves. Fig. 3 shows the trap density dependency of 0.6 eV depth trap with 1 MHz frequency. *C-V* shifts and plateau characteristics depending on the trap densities are successfully observed.

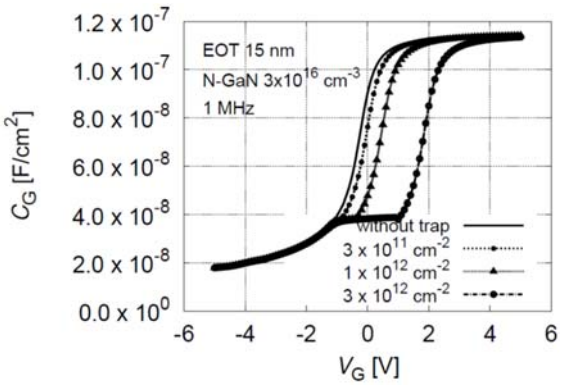

Fig. 3 Trap density dependence of GaN MOS *C-V* curves obtained by the present method for 1 MHz. *C-V* shifts and plateau characteristics are successfully considered.

Fig. 4 shows frequency dispersion of *C-V* curves containing 0.6 eV depth interface traps with the density of 10^{12} cm^{-2} calculated by the present method. Undesirable capacitance peaks are observed larger in lower frequency conditions which is typically observed in measurements.

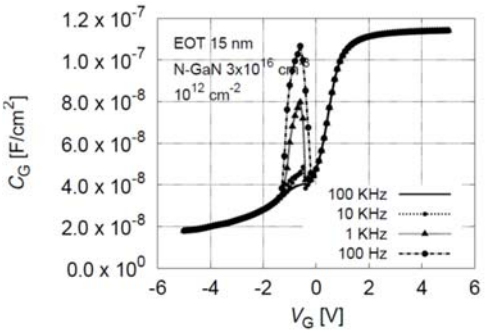

Fig. 4 Frequency dispersion of GaN MOS *C-V* curves obtained by the present method for the density of 10^{12} cm^{-2}. Undesirable capacitance peaks are observed.

Sinusoidal changes of charges of electrons and traps during the simulation steps of each bias points are shown in Fig. 5 for the case of 100 Hz of Fig. 4. For the gate bias of -1 V (a) where increased capacitance is observed, both electron and trap charges change corresponding to the gate bias sine wave. For the gate bias of -0.5 V (b) where the peak capacitance is observed, the trap charge reaches the maximum of 10^{12} cm^{-2}. This is the reason why the capacitance decreases when the gate bias is increased over -0.5 V.

Fig. 6 shows the case of hysteresis of the same measurements in Fig. 4 100 KHz but using faster bias sweep speed. The trapped electrons cannot emit from the deep traps when gate bias is swept from high to low. This is a typical case of hysteresis observed in measurements.

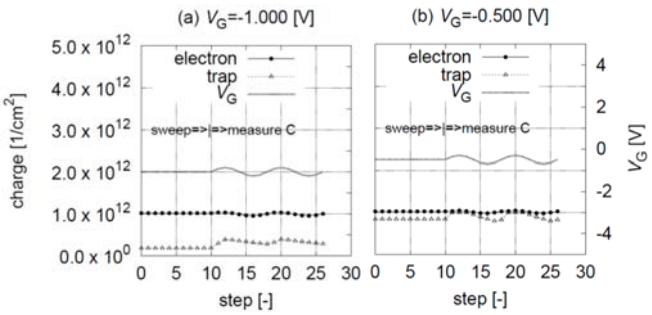

Fig. 5 Internal changes of electrons and traps charge area densities corresponding to the given sign wave gate biases.

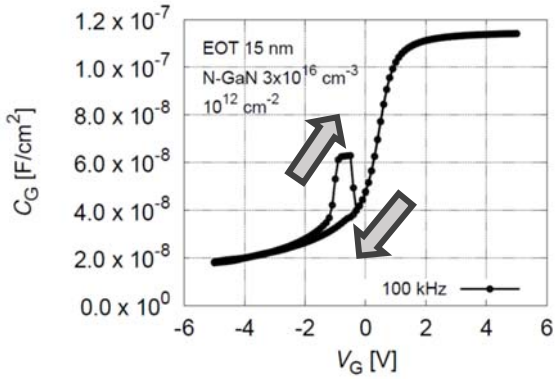

Fig. 6 Hysteresis of C-V curves simulated using slower gate bias sweep speed.

5. Conclusions

A compact model of MOS capacitances taking deep level interface trap effects into account is proposed based on 1-eimensional numerical solver, which solves Poisson, carrier continuity, and trap rate equations consistently by implicit discretization scheme for transient terms. Only several ten's of mesh points are used and the decouple method enables smallest resources considering application in circuit simulation. The proposed approach successfully explain unideal C-V characteristics including plateau, frequency dispersions and hysteresis, and proved to be a powerful modeling tool of GaN MOS capacitors. It is worth mentioning that this method is easily applied to MOS capacitors of other semiconductors.

Acknowledgements

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