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Significant Improvement of p-type 4H-SiC MOS Interface Characteristics by Low Temperature Post-Oxidation Annealing in $H_2O + O_2$ Ambient

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Abstract

We investigated the interface characteristics of p-type 4H-SiC MOS (0001) capacitors fabricated with dry oxidation and post oxidation annealing in $H_2O + O_2$ ambient. We found that these capacitors showed improvement of properties of their interface, as a significant reduction of interface state density, near interface-trap density, fixed charge density.

1. Introduction

Due to the increasing demand for the advanced energy management system, development of integrated circuits on widegap semiconductors for high-temperature operation is attracting more attention. CMOS devices on SiC [1] are strongly expected for the application of data processor or drivers without cooling systems in harsh environment. On 4H-SiC, however, the fabrication technologies of p-channel MOSFETs are still unestablished, even though those of n-channels have been extensively developed for the advanced power device applications. It is generally considered that conventional dry thermal oxidation results in the interface with a huge density of hole traps [2]. The interface nitridation passivation process, which is one of the standard techniques for n-MOSFET fabrication, is also considered to leave those hole traps to cause V_{th} instability against negative bias stress [3].

Recently, we have shown the benefits of combination of high-temperature dry-oxidation followed by post-oxidation annealing in $H_2O + O_2$ ambient (wet-POA) at the temperature as low as 800℃ for the n-channel mobility enhancement on 4H-SiC (0001) Si-face [4]. This is mainly attributed to the reduction of near-interface oxide traps (NITs), due to the relaxation of structural strain in SiO_2 in near interface region [5]. In addition, it is reported that wet oxidation at 1200℃ is effective even for the improvement of p-channel mobility [2]. Therefore, in this study, we will clarify the effects of low-temperature wet-POA on p-type SiC MOS interface characteristics.

2. Experimental

8°-off axis p-type heavily-doped 4H-SiC (0001) Si-face wafers covered with p-type epitaxial layer (acceptor density ~1.3×10^{16}cm^{-3}) were employed in this study. These were oxidized in dry-O_2 at 1300°C to grow ~25 nm-thick SiO_2 films, followed by wet-POA in H_2O:O_2=1:9 ambient at 800℃ for 0 −8hr. Finally Au gate was evaporated on top to fabricate MOS capacitors. Interface state density (D_{it}) was determined by 1MHz-1kHz high-low frequency method. Areal density of NITs was also characterized by photo-CV measurement.

3. Results and Discussions

A significant improvement of interface characteristics was observed on p-type 4H-SiC MOS capacitors by the wet-POA process. In **Fig. 1** the C-V characteristics of the MOS capacitors with different wet-POA time are compared. The capacitor fabricated with wet-POA 8hr resulted in nearly-ideal characteristics, with small frequency dispersion suggesting the small density of interface defects, whereas the sample without POA resulted in miserable ones.

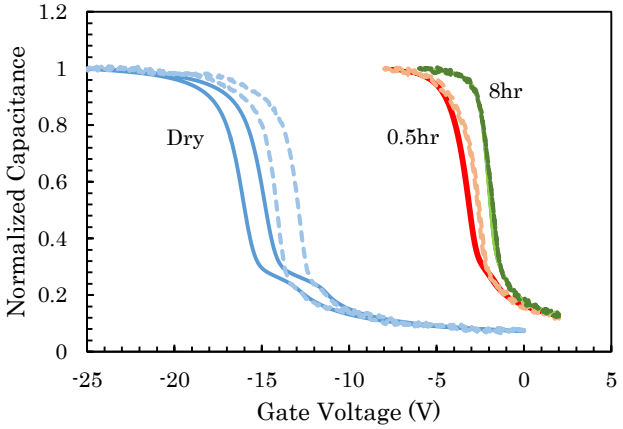

Fig. 1 Normalized C-V characteristics of p-type 4H-SiC MOS capacitors fabricated with different wet-POA time, measured with 1MHz (solid line) and 1 kHz (dotted line).

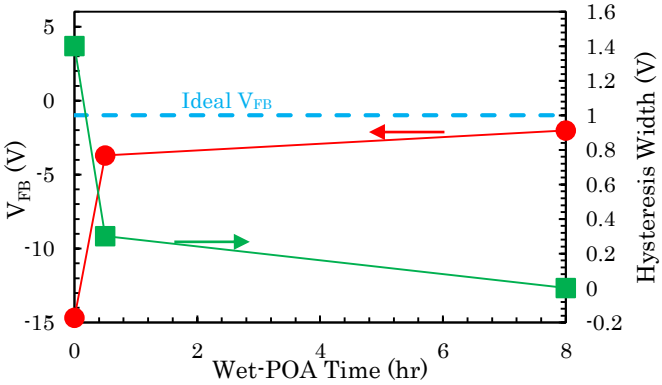

Fig. 2 Wet-POA time dependence of hysteresis width defined with the voltage to give flatband capacitances (left axes) and V_{FB} (right axes). The hysteresis width was defined with the voltage to give flatband

Both the observed flatband voltage (V_{fb}) shift and hysteresis width are plotted as a function of wet-POA time in **Fig. 2**. A huge V_{fb} shift due to significant amount of hole trapping was observed for the sample without POA, however, it recovers closer to the ideal V_{fb} by extending the POA time. The estimated interface fixed charge density was as low as 7.9×

10^{11} cm^{-2} after 8hr POA. The voltage hysteresis was also minimized by the POA to less than 0.1 mV, corresponding to the trap charge density 4×10^7 cm^{-2}.

The observed D_{it} are shown as a function of energy levels in **Fig. 3 (a)**, and the wet-POA time dependence of D_{it} value at the energy of 0.2 eV above valence band edge (E_v) of 4H-SiC is shown in **Fig. 3 (b)**. The significant reduction of D_{it} was clearly observed, and the record-low D_{it} value 2.5×10^{11} $cm^{-2}eV^{-1}$ was achieved by 8hr wet-POA, at the energy level of E_v + 0.2 eV.

Next, NITs with relatively slow time constant was evaluated by photo-CV measurement technique [6,7]. of 4H-SiC In this method, the trapped holes near the interface were once eliminated by electron injection with 3.4 eV light irradiation under inversion voltage. Then the voltage was swept after turning off the light to evaluate the hysteresis of 1MHz C-V curve due to the capturing the holes, as shown in **Fig. 4 (a)** for the case of 8hr wet-POA. From the hysteresis width defined at flatband capacitance (ΔV_{hys}), the areal density of NITs with long time constant was approximately estimated, as shown in **Fig. 4 (b)**. The slow NIT density shows a dramatic reduction by two orders by 8hr wet-POA.

The V_{fb} stability again negative gate bias was also evaluated by applying 3MV/cm constant electric field stress to the MOS capacitors. As shown in **Fig. 5**, the POA for moderate duration (0.5hr) suppressed the V_{fb} shift for 1000 sec, whereas longer wet-POA results in more deterioration of the interface quality. Such drawback of wet-POA indicates the necessity of further improvement of the process conditions.

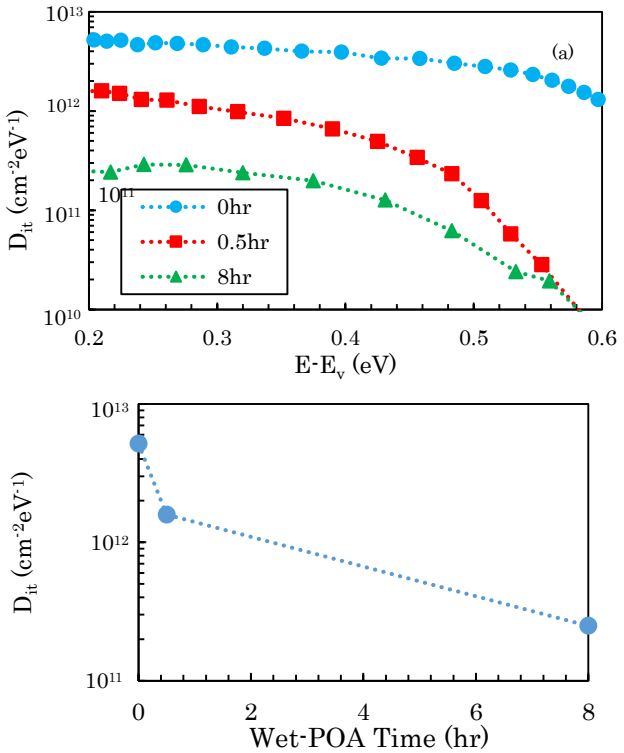

Fig. 3 (a) D_{it} as a function of energy obtained from p-type MOS capacitors fabricated with various wet-POA time by 1MHz-1kHz high-low method. (b) Wet-POA time dependence of D_{it} at the energy level of E_v + 0.2 eV.

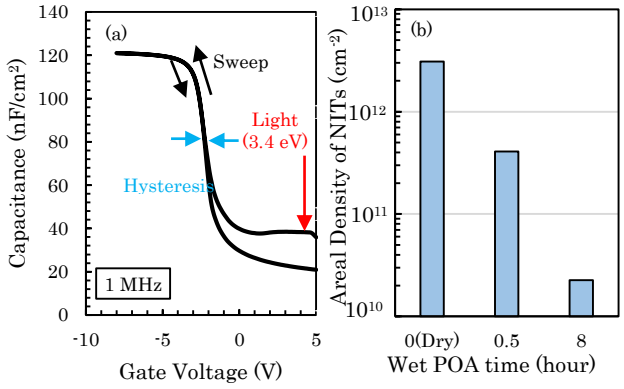

Fig. 4(a) Photo-C-V curves by Photo-assisted measurement for the 8hr wet-POA sample. (b) Areal number density of NITs with long time constant for each sample.

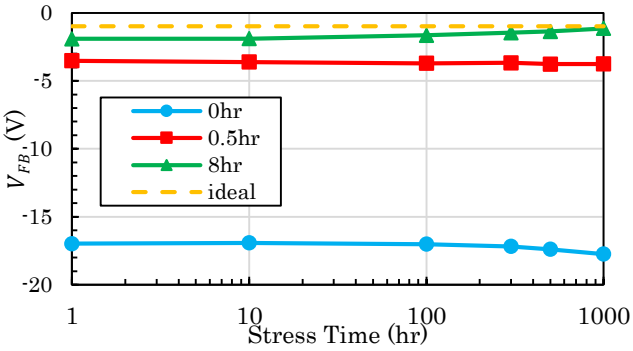

Fig. 5 Stress time dependence of V_{FB} under negative bias of 3 MV/cm. The electric field was defined referring V_{FB} in the initial state. Ideal V_{FB} is indicated by dotted line.

4. Conclusions

A significant improvement of p-type 4H-SiC (0001) MOS interface characteristics was clearly demonstrated by the application of POA process at low temperature in $H_2O + O_2$ ambient, by dramatic reduction of interface defects. Even though further modification of process condition is still desired to improve the instability of V_{FB} against negative bias, H_2O-POA is one of the promising method to provide MOS good quality interface with fewer hole trapping.

Acknowledgements

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