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Diamond pseudo-vertical Schottky barrier diodes fabricated on mosaic wafers

Shinya Ohmagari[1,*], Hideaki Yamada[1], Hitoshi Umezawa[1], Nobuteru Tsubouchi[1], Akiyoshi Chayahara[1], Akinori Seki[2], Fumiaki Kawaii[2], Hiroaki Saitoh[2], and Yoshiaki Mokuno[1]

[1] Diamond Materials Team, Advanced Power Electronics Research Center (ADPERC), National Institute of Advanced Industrial Science and Technology (AIST)
1-8-31, Midorigaoka, Ikeda, Osaka 563-8577, Japan
[2] TOYOTA Motor Corporation,
1 Toyota-cho Toyota City, Aichi 471-0826, Japan
* E-mail: shinya.ohmagari@aist.go.jp, Phone: +81-72-751-7869

Abstract

Diamond mosaic wafers in which several seed crystals are connected laterally by chemical vapor deposition (CVD), are promising large-scale wafers for device integration. High-quality void-free wafers with 40×60 mm^2 were successfully developed. On boundary region where seed substrates are connected, non-uniform crystallinity due to existence of dislocations will cause a degradation device performance. To overcome these drawbacks, we adopted a novel CVD technique to suppress dislocations which normally propagate from substrate to epitaxial layer. In this study, Schottky barrier diodes (SBD) were fabricated on mosaic wafers, and effects of coalescence boundaries on device properties were investigated. The SBD showed excellent rectifying actions after dislocation reduction, on/off ratio over 8 digits, electric field strength of 4 MV/cm, regardless of the existence of boundary.

1. Introduction

With the superlative physical properties of a high breakdown field exceeding 10 MV cm^{-1}, high carrier mobility (electron 7300, hole 5300 cm^2 V^{-1} s^{-1}) [1], and high thermal conductivity (22 W cm^{-1} K^{-1}), single-crystal diamond has attracted much attention as a material for next-generation low-loss power devices [2], [3]. High switching capabilities have been demonstrated for both unipolar and bipolar devices, Schottky rectifiers [4], [5], p-i-n diodes [6], and field-effect transistors (FETs) [7], [8]. For the device integration, large-scale wafers at least several inches are necessary, however, for diamond, the typical crystal size of commercially-available substrate is only several millimeters that hampers industrial applications.

Recently, diamond mosaic wafers in which several seed crystals are connected laterally by chemical vapor deposition (CVD) has been developed. By using *clone wafers* which are freestanding substrates duplicated from one identical seed crystals via ion-implantation and lift-off processes, void-free high-quality wafers with 40×60 mm^2 were successfully fabricated [9]. One of the most important concerns is crystallographic non-uniformity due to existence of coalescence boundaries [10]. The large number of threading dislocations are exist that cause a degradation of device performance.

More recently, we have developed a novel CVD process to annihilate threading dislocation (TD) which normally propagate from substrate to epitaxial layer [11]. Owing to the dislocation reduction, device performances were improved: a significant enhancement of breakdown strength with decreased leakage current has demonstrated. In this study, pseudo-vertical SBD were fabricated on mosaic wafers by adopting aforementioned CVD process.

2. Experimental

Diamond mosaic wafers (100) substrates with its size of 20×30 mm^2 comprising six pieces of original seed crystals were used as substrates. Firstly, a heavily boron-doped conductive layer was epitaxially grown by hot-filament CVD [12]. The B concentration and film thickness were 1.8×10^{20} cm^{-3} and 4.9 μm, respectively. The cross-sectional cathodoluminescence image revealed that propagation of dislocation was largely suppressed at this HFCVD layer. The detailed suppression mechanism of threading dislocation will be elucidated elsewhere. Then, lightly B-doped drift layer with its B concentration and thickness of 2.9×10^{17} cm^{-3} and 3.3 μm were deposited. In order to investigate the effects of coalescence boundaries, 200 Schottky contacts with diameter of 100 μm were fabricated by photolithography and lift-off process. Mo/Au Schottky and Ti/Mo/Au Ohmic electrodes were deposited by EB evaporator. The current-voltage characteristics were evaluated at room temperature using semiconductor power analyzer (Agilent Technologies B1505A).

3. Results and discussion

Figure 1 shows differential interference-contrast optical microscopy image of SBDs fabricated on mosaic wafers.

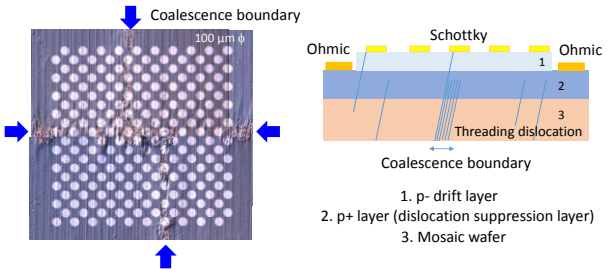

Fig. 1. Pseudo-vertical SBDs fabricated on mosaic wafers near coalescence boundary. The right figure shows schematic cross-sectional view.

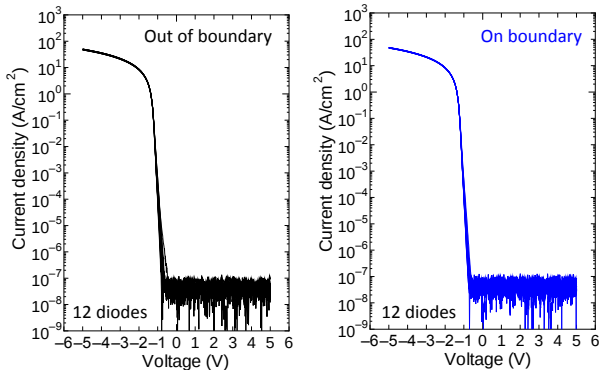

Fig. 2. I-V characteristics of SBDs fabricated near coalescence boundaries of diamond mosaic wafers.

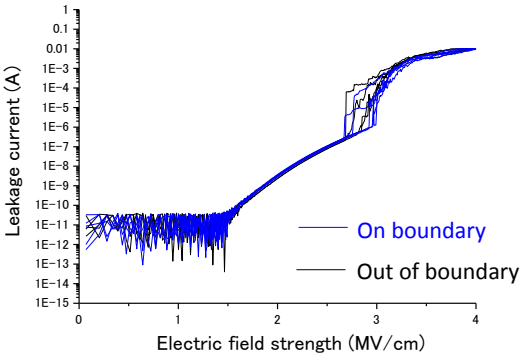

Fig. 3. Reverse-voltage characteristics of SBDs fabricated near coalescence boundaries.

Number of Schottky electrodes were deposited around coalescence boundary. The schematic cross-sectional view is also shown in the right. Our preliminary results showed that large leakage current accompanied with degraded ideality factor (n) and Schottky barrier height (ϕ_B) was confirmed near or just above boundaries due to dislocations. Contrary, it has been demonstrated that a large number of TD is significantly suppressed into layer 2, HFCVD-grown p+ films.

Figure 2 exhibits I-V characteristics of SBDs. The diodes exhibited high rectification ratio over 10^8 and low leakage current below the detection limit of our apparatus, regardless of the existence of boundaries. These I-V curves comprising 12 diodes showed near identical characteristics: n and ϕ_B values extracted from thermionic emission model are almost equivalent. Although the non-uniformity of diode properties are commonly observed even 3×3 mm^2 substrate, our device showed homogenous distribution.

Figure 3 shows the reverse-voltage characteristics. The leakage current was steeply increased from reverse voltage strength above 1.4 MV/cm, and breakdown behavior was observed at 2.7-3.1 MV/cm with sudden increase of current. The field plate or guard ring to relieve electric field concentration were not applied, and breakdown points will slightly change after reconstruction of SBD electrodes. This indicates that high electric field was presumably concentrated at roughened diamond surface and Schottky metals which caused by polishing damage. The maximum electric field strength (E_{max}) of 4 MV/cm was observed at relatively smooth diamond surface. Further improvement of E_{max} could be expected by appropriate surface treatments. The high E_{max} and better uniformity of SBD characteristics ensures the mosaic wafers to be applicable for device-ready substrates.

4. Conclusions

Pseudo-vertical SBDs were fabricated on diamond mosaic wafers and effects of coalescence boundaries were investigated. We adopted a novel CVD technique to annihilate TDs which normally propagate from substrate to epilayer. Owing to the TDs reduction, SBD performances were improved. High rectification ratio over 10^8 and low leakage current could be observed, regardless of the existence of boundaries. The forward/reverse characteristics showed identical I-V curves, indicating the homogeneous properties of SBDs.

Acknowledgements

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