Extended Abstracts of the 2018 International Conference on Solid State Devices and Materials, Tokyo, 2018, pp275-276

# Advances in InP Double Heterojunction Bipolar Transistors (INVITED)

Colombo R. Bolognesi,[1] Akshay M. Arabhavi,[1] Wei Quan,[1] Olivier Ostinelli,[1] Xin Wen[2] and Mathieu Luisier[2]

[1] Millimeter-Wave Electronics Group
ETH-Zürich,
CH-8092 Zurich, Switzerland
Phone: +41-44-632-8775, E-mail: colombo@ieee.org
[2] Integrated Systems Laboratory
ETH-Zürich,
CH-8092 Zurich, Switzerland

**Abstract**

**Double Heterojunction Bipolar Transistors (DHBTs) are intended to extend the breakdown voltage beyond what is possible in single heterojunction bipolar transistors (sHBTs), ideally without sacrificing frequency performance. The present paper contrasts the various approached to the realization of InP DHBTs. Technological evolution over the last two decades suggests that base transport properties take a secondary role to the ease of electron transfer from the base to the wide-bandgap collector material.**

## 1. Introduction

The idea of separately optimizing the base and collector in bipolar transistors with a double heterojunction architecture was raised several years ago [1] but remained largely unexploited for GaAs-based devices. GaAs sHBTs have proven hugely successful commercially but offer relatively low cutoff frequencies. The evolution toward higher operating speeds pushed cutting edge device R&D activities toward InP-based materials, but unfortunately, InP/GaInAs sHBTs showed approximately the same $f_T \times BV_{CEO}$ = 650 GHz-V product as GaAs sHBTs because of the low breakdown fields and poor high-field transport properties of $Ga_{0.47}In_{0.53}As$ collectors. This limitation motivated the development of InP-based DHBTs with the to exploit the short base transit times associated with GaInAs and the high-breakdown fields and favorable transport properties of InP collector layers. In order to do this, the B/C heterojunction must be designed to prevent blocking of the collector current. Two types of grading schemes have been developed for GaInAs, namely the step-graded launcher [2] and the chirped-superlattice collector [3]. An alternative to these designs relying on the “Type-II” InP/GaAsSb system has been developed since 1997 in our group [4].

## 2. DHBT Architectures

*Inroduction*

The need to avoid electron blocking at the interface between the narrow gap base and widegap collector was already raised in Kroemer`s classic paper [1] which stated: “*It is important that the free collection of electrons by the reverse-biased collector not be impeded by any heterobarrier due to a conduction band discontinuity. Such barriers are easily eliminated by grading the heterostructucture*.” Kroemer recognized the importance of blocking-free collection and anticipated that modern epitaxial growth techniques would allow the realization of effective compositional grading schemes, but did not consider the effects of high current densities on the self-consistent potential collector profile, and that transistor operation can drive devices to low collector voltages (and even forward bias the B/C junction). The resulting collapse of the electric field leads to current blocking in an otherwise adequately graded B/C heterojunction. This work considers below the salient features of each collector structure.

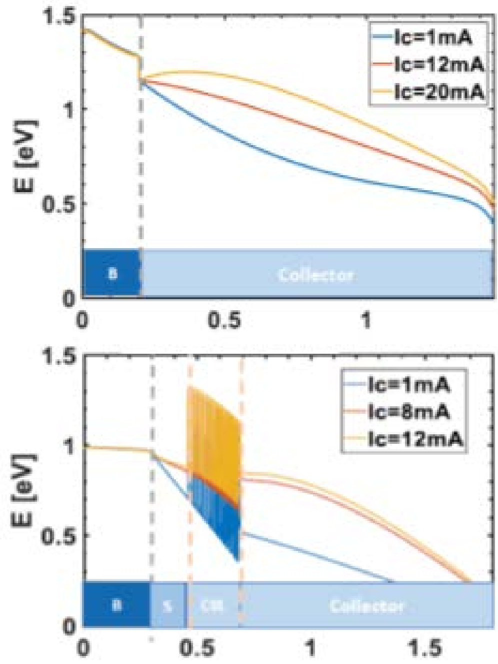


Fig. 1 Self-consistent band diagrams for different collector current levels for a Type-II abrupt collector (top) contrasted to that of a CSL collector with a GaInAs base. High current space charge effects result in blocking when a GaInAs base is used.

*Step-Graded Launcher*

In a step-graded collector, the narrow-gap GaInAs base material is extended into the collector region in order to allow electrons to gain enough kinetic energy to overcome the conduction band discontinuity with InP. More than one compositional steps maybe use to facilitate the transition. The inherent shortcoming of this approach is associated with the presence of a peak in electric field in the minimum bandgap GaInAs setback layer near the base region. Breakdown voltages are limited by interband tunneling in the setback GaInAs layer.

*CHIRP Superlattice (CSL) Collector*

In the so-called CHIRP superlattice collector, the compositional grading to InP is accomplished through a variable duty cycle short period superlattice. CHIRP in fact stands for "coherent heterointerfaces for reflection and penetration," and was originally a structure intended to achieve negative differential resistance [5]. In the best case scenario under a bias resulting in full alignment of the miniband, transport can simply not be better than in bulk GaInAs because minibands necessarily feature flattened *E vs. k* dispersion relations compared to bulk GaInAs. Next, voltage and current swings tend to bring the minibands out of resonance, disrupting current flow as shown in Fig. 1. When a GaInAs setback layer is used near the base, the CSL shares the short-coming of the step-graded collector, *i.e.* a tunneling-limited low breakdown voltage.

*Type-II Staggered Launcher*

The Type-II staggered launcher uses a GaAsSb (or more recently GaInAsSb) base layer forming an abrupt staggered junction with the InP collector in such a way that the base conduction band lies above that of InP. Our Group largely pioneered this approach since 1997, first in Canada and then at ETH-Zürich. InP/GaAsSb DHBTs have now been shown with maximum oscillation frequencies exceeding 1.1 THz [6] per conventional de-embedding methods. Whereas GaAsSb base layers have a lower electron mobility than GaInAs, InP/GaAsSb DHBTs show higher current gain cutoff frequencies $f_T$ than GaInAs based devices with a comparable $f_{MAX}$ and/or base and collector thicknesses.

## 3. Simulations

*Inroduction*

To understand the aforementioned observations, the three types of base/collector designs were simulated in a quantum transport device simulator (OMEN [7]) based on the empirical nearest-neighbor tight-binding method to understand how electrons move from the base (GaInAs or GaAsSb) to the InP collector. The calculations use accurate *ab initio* atomistic band structures rather than back-of-the-envelope Γ-valley band edge profiles interpolated from the binary components, and quantum transport as opposed to the classical drift/diffusion techniques used in commercial TCAD simulators (which only account for the density-of-states effective masses and carrier mobilities/diffusivities, whereas details about different energy band valleys, their proximity, and interactions are simply omitted, as are quantum mechanical reflections at potential barriers).

Various collector designs were simulated in order to understand the involved trade-offs. Whereas all collectors show a decreased performance at high current densities that can loosely be attributed to the Kirk effect as seen in Fig. 1, transport in the Type-II collector is clearly less strongly affected by high-current effects. As one might expect from the Type-II band diagram in Fig. 1, the electron velocity is least sensitive to the collector current density in the InP/GaAsSb system —it also results in the shortest simulated base/collector delay time. In contrast, the CSL band diagram results in severe perturbation for the electron collection as current increases which has been related to device nonlinearities.

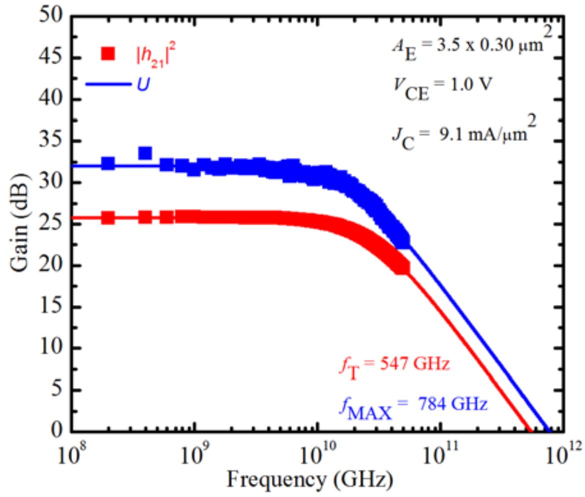


Fig. 2 Measured RF performance of a 0.3 × 3.5 μm$^2$ emitter quaternary graded-base InP/GaInAsSb DHBT. To our knowledge, this is the highest $f_T$ ever achieved in a DHBT with $f_{MAX} > f_T$.

## 4. Recent Experimental Advancements

*InP/GaAsSb and InP/GaInAsSb DHBTs*

Recent work has focused on achieving a better understanding of device operation and optimizing frequency performance in ternary and quaternary base DHBTs. Fig. 2 gives the RF performance of a quaternary graded-base device showing the best performance ever achieved in a quaternary base DHBT. To the best of our knowledge it is also the highest $f_T$ for a DHBT with $f_{MAX} > f_T$.

## 5. Conclusions

Our conference presentation will expand on these findings and their interpretation. The simulations will be used to highlight the fundamental limitations of InP/GaInAsSb DHBTs.


## Acknowledgements

We would like to acknowledge support from the Swiss National Science Foundation and ETH for partial support. We thank the FIRST Cleanroom Laboratory personnel for their support.


## References


[1] H. Kroemer, Proc. IEEE **73** (1982) 13.
[2] Y. Matsuoka *et al*., Jpn. J. Appl. Phys. **35** (1996) 5646.
[3] C. Nguyen *et al*., IEEE Electron Dev. Lett. **17** (1996) 133.
[4] C.R. Bolognesi, IEEE Electron Dev. Lett. **20** (1999) 155.
[5] T. Nakagawa *et al*., Electronics Lett. **19** (1983) 822.
[6] P. Chevalier *et al*., Proc. IEEE **105** (2017) 1035.
[7] M. Luisier *et al*., Phys. Rev. B **74**, (2006) 205323.