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Low leakage current and High mobility Ultra-thin-body InGaSb p-FETs

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Abstract

We demonstrated low leakage current and high mobility ultra-thin body (UTB) (In)GaSb p-FETs with $In_{0.53}Ga_{0.47}As$ surface passivation, and GaSb/InGaSb/GaSb quantum well (QW) channel structure. The fabricated devices showed the lowest off-leakage current (I_{off}), subthreshold slope (*S.S.*) and high effective mobility (μ_{eff}) among reported GaSb p-FETs.

1. Introduction

Antimonide(Sb)-based III-V compounds are promising materials for future high performance logic, radio frequency (RF), as well as low power devices [1,2]. Although the potential of these materials has been reported by many groups, the progress of FETs using these materials is quite slow and number of reports is quite few compared to other III-V materials, which is mainly caused by difficult material growth and material control during device fabrication process. Moreover, MOS interface control is extremely difficult, which makes μ_{eff} lower and I_{off} higher. From these reasons, typical GaSb-based transistors have technological issues such as large I_{off} (including bulk buffer leakage and surface leakage through interface traps) and low μ_{eff} due to large D_{it}, as shown in Fig. 1(a). Indeed, typical I_{off} of reported GaSb pFET is quite large even for long channel devices [3-15].

To solve these issues, in this study, we demonstrate the UTB (In)GaSb p-FET using novel barrier, MOS interface, and channel engineerings, summarized in Fig. 1(a). First, in order to form good MOS interface and reduce interface trap-assisted surface leakage, we introduced the $In_{0.53}Ga_{0.47}As$ (InGaAs) surface passivation on (In)GaSb channel layers because InGaAs has a proper band offset to confine hole at high-quality epitaxial interface between InGaAs and (In)GaSb. Moreover, a good interfacial quality is expected utilizing lower D_{it} at mid gap to valence band in $Al_2O_3/In_{0.53}Ga_{0.47}As$ compared to lattice-matched InAs passivation, which has been much studied to passivate GaSb [9,10]. Finally, we introduced compressively strained $In_{0.25}Ga_{0.75}Sb$ QW channel to enhance the mobility by using channel strain and reducing coulomb scattering and thickness-fluctuation scattering [10-12]. Through these engineering, we demonstrated high-performance (In)GaSb p-FETs showing remarkably low I_{off}, *S.S.*, and high μ_{eff}.

2. Fabrication of (In)GaSb UTB pFET

First, we grew the epitaxial structure for InGaSb pFETs. Epitaxial layers of 1.5-nm-thick InGaAs/5-nm-thick GaSb/5-nm-thick InGaSb/5-nm-thick GaSb/950-nm-thick AlGaSb were grown on (100) S.I. GaAs substrates by MBE. For GaSb single channel FETs, 15-nm-thick GaSb was grown instead of 5-nm-thick GaSb/5-nm-thick InGaSb/5-nm-thick GaSb QW.

Using this wafer, we fabricated InGaSb pFET following the process in Fig. 1(b). First, we carried out the pre-treatment for InGaAs surface and deposited 5-nm-thick Al_2O_3 as a gate oxide using ALD. Then, each device was isolated by mesa etching and S/D was formed using Pt. Finally, 10-nm-thick Al_2O_3 and Pt gate was formed, followed by rapid thermal annealing (RTA). Cross-sectional TEM images of this sample are shown in Fig. 2 (a)-(b), indicating the excellent crystal quality of channel layer and the abrupt interfaces between each material. Fast Fourier transform (FFT) pattern of channel and EDX mapping profile also confirms single crystalline behaviors without any identifiable morphological defects and its material compositions.

3. Characterization of the fabricated (In)GaSb UTB pFETs

We investigated the impact of the surface pre-treatment as shown in Fig. 3, indicating the transfer curve is significantly improved by HF(1%) surface cleaning, which would be attributed to low D_{it} at mid gap to valence band in HF-treated Al_2O_3/InGaAs interface [8] and chemically stable HF-treated InGaAs surface than Ammonia-based solutions-treated surface. To investigate the impact of InGaAs passivation, we compared transfer curves of the GaSb pFET with and without InGaAs passivation in Fig. 4. InGaAs passivation shows much improvement both in I_{on}, I_{off}, and *S.S.* characteristics. Fig. 5 shows excellent I_{DS}-V_{GS} and I_{DS}-V_{DS} curves of the GaSb p-FET with InGaAs passivation, RTA at 250ºC, gate length (L_g) = 5 μm, showing small *S.S.* of 198 mV/dec, high I_{on}/I_{off} ratio of 2.3×10^3, and clear current saturation in output curve. This was obtained by InGaAs passivation and proper thermal treatment, as shown in Fig. 6. First, all performance metrics (I_{off}, *S.S.*, I_{on}/I_{off}, μ_{eff}) improve with increasing RTA temperature at relatively low temperature range, indicating the improvement of Al_2O_3/InGaAs interfacial properties by RTA. However, off-state behavior (I_{off}, *S.S.*, I_{on}/I_{off}) degrades with RTA at higher than 300 °C, whereas μ_{eff} constantly increases with increasing RTA temperature up to at least 310ºC. These results indicate that the degradation of off-state characteristics is probably originated from junction degradation rather than D_{it} increase. Therefore, further improvement is still possible by process modification. In present study, to achieve balanced on- and off-state characteristics, we used RTA at 250 °C in other devices. As described earlier, to further enhance μ_{eff}, we introduced GaSb/InGaSb/GaSb QW structure. Fabricated InGaSb QW p-FETs with InGaAs passivation shows well-behaved *I-V* curves, as shown in Fig. 7 with significantly enhanced I_{on} compared to GaSb p-FETs in Fig. 7, while maintaining I_{off} low. Fig. 8 shows the large improvement in μ_{eff} in InGaSb QW p-FET at whole N_s range compared to GaSb p-FETs. InGaSb QW p-FETs show the high μ_{eff} of 176 cm^2/Vs, which is 1.7 times higher than GaSb channel. Since off-state characteristics can degrade *S.S.* (not only by D_{it}) (Fig. 6), D_{it} extraction from *S.S.* value may not always provide correct D_{it}. Therefore, to eliminate the effect of I_{off} and extract D_{it} in our devices, we investigated the temperature dependence of *S.S.*. Temperature dependence of *S.S.* is shown in Fig. 9. Calculated *S.S.* with D_{it} for our device is also shown. At higher temperature than 250K, *S.S.* shows the sharp increase with increasing temperature, indicating that I_{off} degrades *S.S.* and it hinders extracting the correct *S.S.* decided by D_{it}. On the other hand, at low temperature, *S.S.* follows the calculated *S.S.* with D_{it} of 10^{11} $eV^{-1}cm^{-2}$, because I_{off} does not impact anymore due to sufficiently lowered I_{off} at low temperature. It should be noted that obtained D_{it} is exceptionally low for GaSb-based devices. These results strongly indicate that the MOS interface is significantly improved by InGaAs passivation. Furthermore, *S.S.* is expected to be further improved by scaling EOT and further reducing D_{it}. To qualify the S/D junction and limiting factor of I_{off}, we extracted activation energy (E_a) of I_{off}, as in Fig. 10. Extracted E_a was found to be lower than half of bandgap of GaSb channel, indicating I_{off} is affected by trap-assisted transport and/or surface leakage at present devices. Improvement in crystal quality and process optimization will provide further improvement in the device performance. InGaSb QW

p-FETs also showed similar tendency in *S.S.* and E_a (not shown). Fig 11 shows the benchmark of $I_{off} - V_D$ and $\mu_{eff} - I_{on}/I_{off}$ in GaSb and InGaSb p-FETs reported so far [1-15]. We found that our UTB (In)GaSb p-FETs with InGaAs passivation significantly enhanced the device performance at off-state characteristics as well as on-state characteristics.

4. Conclusion

We successfully demonstrated (In)GaSb p-FETs with low I_{off}, *S.S.*, and high μ_{eff} via optimization of insulating barrier, introduction of InGaAs passivation and QW channel structure. Our devices showed nearly record-performance in $I_{off} - V_D$ and $\mu_{eff} - I_{on}/I_{off}$ among reported GaSb-based devices.

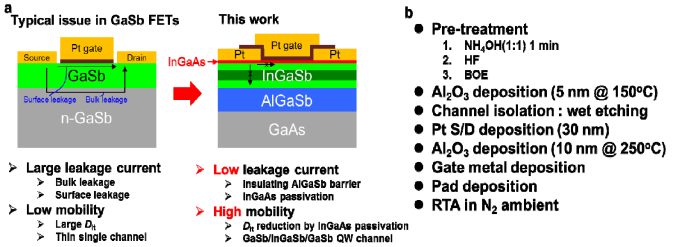

Fig. 1 (a) Schematic image of GaSb pFET and its typical technological issues and our approach to solve these issues. (b) Fabrication process flow.

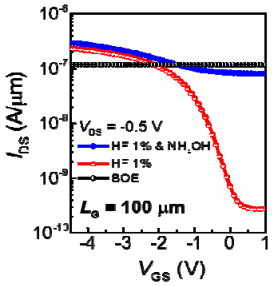

Fig. 3 Impact of the pre-treatment before Al_2O_3 deposition.

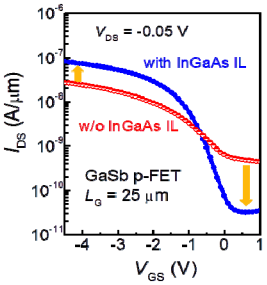

Fig. 4 Transfer curve of GaSb pFET w/ and w/o InGaAs passivation.

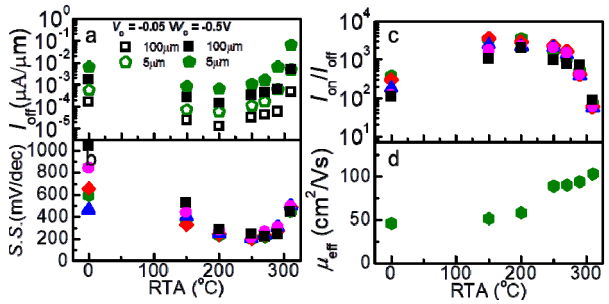

Fig. 6 RTA temperature dependence of (a) I_{off}, (b) *S.S.*, (c) I_{on}/I_{off}, and (d) μ_{eff} characteristics of GaSb p-FET with InGaAs passivation.

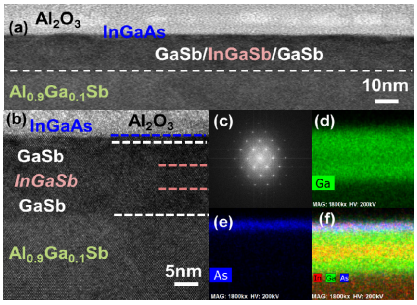

Fig. 2 (a) Cross-sectional TEM image and (b) HR image and (c) FFT pattern of channel and its EDX mapping image of (d) Ga (e) As (f) In, Ga, As.

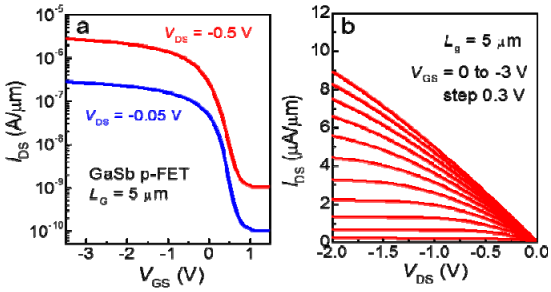

Fig. 5 (a) $I_{DS} - V_{GS}$ curves of GaSb p-FET with InGaAs passivation, RTA at 250°C, L_g= 5 μm (b) output characteristics.

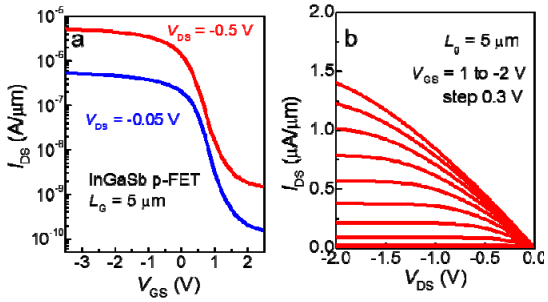

Fig. 7 (a) I_{DS}–V_{GS} curves of the (In)GaSb QW p-FET with InGaAs passivation, L_g= 5 μm and (b) output characteristics.

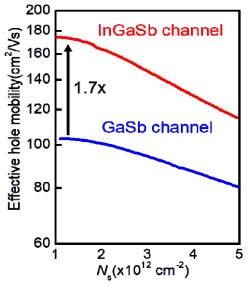

Fig. 8 $\mu_{eff} - N_s$ of the GaSb and InGaSb QW p-FETs.

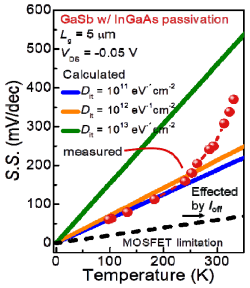

Fig. 9 T dependence of *S.S.* Calculated line and measured data.

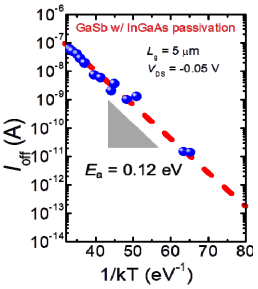

Fig. 10 T dependence of I_{off} of GaSb pFET with InGaAs passivation.

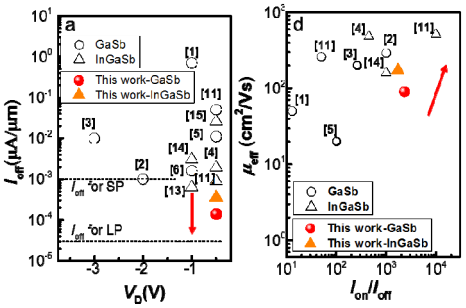

Fig. 11 Benchmarks of (a) $I_{off} - V_D$, (b) $\mu_{eff} - I_{on}/I_{off}$ in GaSb and InGaSb p-FETs. Red arrows show the technology development direction

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